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=> FILE HOME
FILE 'HOME' ENTERED AT 18:52:57 ON 20 JAN 2011


=> DISPLAY HISTORY FULL L1-

     FILE 'HCA, WPIX, JAPIO' ENTERED AT 15:53:17 ON 20 JAN 2011
L1        449921 SEA (SILICON OR SI OR SILICA# OR SIO2 OR SEMICOND? OR
                 SEMI(A)(COND# OR CONDUCT?))(3A)(WAFER? OR DISK? OR DISC##
                 OR PLATE OR PLATES OR SHEET? OR SUBSTRAT? OR SURFACE? OR
                 BASE OR BASES OR FOUNDATION? OR SUBSTRUCT? OR UNDERSTRUCT?
                 OR UNDERLAY? OR PANE?)
L2        416207 SEA (SILICON OR SI OR SILICA# OR SIO2 OR SEMICOND? OR
                 SEMI(A)(COND# OR CONDUCT?))(3A)(WAFER? OR DISK? OR DISC##
                 OR PLATE OR PLATES OR SHEET? OR SUBSTRAT? OR SURFACE? OR
                 BASE OR BASES OR FOUNDATION? OR SUBSTRUCT? OR UNDERSTRUCT?
                 OR UNDERLAY? OR PANE?)
L3        203474 SEA (SILICON OR SI OR SILICA# OR SIO2 OR SEMICOND? OR
                 SEMI(A)(COND# OR CONDUCT?))(3A)(WAFER? OR DISK? OR DISC##
                 OR PLATE OR PLATES OR SHEET? OR SUBSTRAT? OR SURFACE? OR
                 BASE OR BASES OR FOUNDATION? OR SUBSTRUCT? OR UNDERSTRUCT?
                 OR UNDERLAY? OR PANE?)
     TOTAL FOR ALL FILES
L4       1069602 SEA (SILICON OR SI OR SILICA# OR SIO2 OR SEMICOND? OR
                 SEMI(A)(COND# OR CONDUCT?))(3A)(WAFER? OR DISK? OR DISC##
                 OR PLATE OR PLATES OR SHEET? OR SUBSTRAT? OR SURFACE? OR
                 BASE OR BASES OR FOUNDATION? OR SUBSTRUCT? OR UNDERSTRUCT?
                 OR UNDERLAY? OR PANE?)
L5         16014 SEA MONOCRYST? OR MONO(2A)CRYST?
L6         16913 SEA MONOCRYST? OR MONO(2A)CRYST?
L7          2373 SEA MONOCRYST? OR MONO(2A)CRYST?
     TOTAL FOR ALL FILES
L8         35300 SEA MONOCRYST? OR MONO(2A) CRYST?
L9        575968 SEA LAMEL? OR LAMIN? OR MULTILAYER? OR MULTIFILM? OR
                 MULTICOAT? OR (MULTI OR MULTIPL? OR PLURAL? OR SEVERAL OR
                 NUMEROUS? OR FEW OR MANY OR MANIFOLD? OR MULTIFOLD? OR
                 MULTITUD?)(2A)(LAYER? OR COAT? OR FILM?)
L10       523993 SEA LAMEL? OR LAMIN? OR MULTILAYER? OR MULTIFILM? OR
                 MULTICOAT? OR (MULTI OR MULTIPL? OR PLURAL? OR SEVERAL OR
                 NUMEROUS? OR FEW OR MANY OR MANIFOLD? OR MULTIFOLD? OR
                 MULTITUD?)(2A)(LAYER? OR COAT? OR FILM?)
L11       333113 SEA LAMEL? OR LAMIN? OR MULTILAYER? OR MULTIFILM? OR
                 MULTICOAT? OR (MULTI OR MULTIPL? OR PLURAL? OR SEVERAL OR
                 NUMEROUS? OR FEW OR MANY OR MANIFOLD? OR MULTIFOLD? OR
                 MULTITUD?)(2A)(LAYER? OR COAT? OR FILM?)
     TOTAL FOR ALL FILES
L12      1433074 SEA LAMEL? OR LAMIN? OR MULTILAYER? OR MULTIFILM? OR
                 MULTICOAT? OR (MULTI OR MULTIPL? OR PLURAL? OR SEVERAL OR
                 NUMEROUS? OR FEW OR MANY OR MANIFOLD? OR MULTIFOLD? OR
                 MULTITUD?)(2A)(LAYER? OR COAT? OR FILM?)
L13        84538 SEA SANDWICH? OR TRILAYER? OR TRIFILM? OR TRICOAT? OR
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               THREEPLY? OR THREEPLIED OR THREEPLIES OR (TRI OR TRIPL? OR
               TREBL?)(2A)(FILM? OR LAYER? OR COAT?) OR TRIPLEPLY? OR
               TRIPLEPLIED OR TRIPLEPLIES OR TRIPLEPLYING# OR (TRIPL? OR
               THREE OR 3)(A)(PLY OR PLIED OR PLIES OR PLYING#)
L14      69208 SEA SANDWICH? OR TRILAYER? OR TRIFILM? OR TRICOAT? OR
               THREEPLY? OR THREEPLIED OR THREEPLIES OR (TRI OR TRIPL? OR
               TREBL?)(2A)(FILM? OR LAYER? OR COAT?) OR TRIPLEPLY? OR
               TRIPLEPLIED OR TRIPLEPLIES OR TRIPLEPLYING# OR (TRIPL? OR
               THREE OR 3)(A)(PLY OR PLIED OR PLIES OR PLYING#)
L15      48474 SEA SANDWICH? OR TRILAYER? OR TRIFILM? OR TRICOAT? OR
               THREEPLY? OR THREEPLIED OR THREEPLIES OR (TRI OR TRIPL? OR
               TREBL?)(2A)(FILM? OR LAYER? OR COAT?) OR TRIPLEPLY? OR
               TRIPLEPLIED OR TRIPLEPLIES OR TRIPLEPLYING# OR (TRIPL? OR
               THREE OR 3)(A)(PLY OR PLIED OR PLIES OR PLYING#)
     TOTAL FOR ALL FILES
L16     202220 SEA SANDWICH? OR TRILAYER? OR TRIFILM? OR TRICOAT? OR
               THREEPLY? OR THREEPLIED OR THREEPLIES OR (TRI OR TRIPL? OR
               TREBL?)(2A)(FILM? OR LAYER? OR COAT?) OR TRIPLEPLY? OR
               TRIPLEPLIED OR TRIPLEPLIES OR TRIPLEPLYING# OR (TRIPL? OR
               THREE OR 3)(A)(PLY OR PLIED OR PLIES OR PLYING#)
L17       1322 SEA (PHOSPHORUS# OR P)(5A)(DOPE# OR DOPING# OR DOPANT?)(5A)
               (SILICA# OR SIO2 OR (SILICON OR SI)(A)(OXIDE# OR DIOXIDE#))
L18        507 SEA (PHOSPHORUS# OR P)(5A)(DOPE# OR DOPING# OR DOPANT?)(5A)
               (SILICA# OR SIO2 OR (SILICON OR SI)(A)(OXIDE# OR DIOXIDE#))
L19         88 SEA (PHOSPHORUS# OR P)(5A)(DOPE# OR DOPING# OR DOPANT?)(5A)
               (SILICA# OR SIO2 OR (SILICON OR SI)(A)(OXIDE# OR DIOXIDE#))

     TOTAL FOR ALL FILES
L20       1917 SEA (PHOSPHORUS# OR P)(5A)(DOPE# OR DOPING# OR DOPANT?)(5A)
               (SILICA# OR SIO2 OR (SILICON OR SI)(A)(OXIDE# OR DIOXIDE#))
L21       8886 SEA PSG OR PHOSPHOSILICATE# OR PHOSPHO?(A)SILICATE#
L22       3964 SEA PSG OR PHOSPHOSILICATE# OR PHOSPHO?(A)SILICATE#
L23       4254 SEA PSG OR PHOSPHOSILICATE# OR PHOSPHO?(A)SILICATE#
     TOTAL FOR ALL FILES
L24      17104 SEA PSG OR PHOSPHOSILICATE# OR PHOSPHO?(A) SILICATE#
L25        998 SEA (BORON# OR B)(5A)(DOPE# OR DOPING# OR DOPANT?)(5A)(SILI
               CA# OR SIO2 OR (SILICON OR SI)(A)(OXIDE# OR DIOXIDE#))
L26        452 SEA (BORON# OR B)(5A)(DOPE# OR DOPING# OR DOPANT?)(5A)(SILI
               CA# OR SIO2 OR (SILICON OR SI)(A)(OXIDE# OR DIOXIDE#))
L27         40 SEA (BORON# OR B)(5A)(DOPE# OR DOPING# OR DOPANT?)(5A)(SILI
               CA# OR SIO2 OR (SILICON OR SI)(A)(OXIDE# OR DIOXIDE#))
     TOTAL FOR ALL FILES
L28       1490 SEA (BORON# OR B)(5A)(DOPE# OR DOPING# OR DOPANT?)(5A)(SILI
               CA# OR SIO2 OR (SILICON OR SI)(A)(OXIDE# OR DIOXIDE#))
L29       5405 SEA BPSG OR BOROPHOSPHOSILICATE# OR BORO?(3A)PHOSPHO?(3A)SI
               LICATE# OR (BOROPHOSPHO? OR PHOSPHOBORO?)(2A)SILICATE# OR
               BORO?(2A)PHOSPHOSILICATE# OR PHOSPHO?(2A)BOROSILICATE#
L30       3767 SEA BPSG OR BOROPHOSPHOSILICATE# OR BORO?(3A)PHOSPHO?(3A)SI
               LICATE# OR (BOROPHOSPHO? OR PHOSPHOBORO?)(2A)SILICATE# OR
               BORO?(2A)PHOSPHOSILICATE# OR PHOSPHO?(2A)BOROSILICATE#
L31       1531 SEA BPSG OR BOROPHOSPHOSILICATE# OR BORO?(3A)PHOSPHO?(3A)SI
               LICATE# OR (BOROPHOSPHO? OR PHOSPHOBORO?)(2A)SILICATE# OR
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              BORO?(2A)PHOSPHOSILICATE# OR PHOSPHO?(2A)BOROSILICATE#
     TOTAL FOR ALL FILES
L32        10703 SEA BPSG OR BOROPHOSPHOSILICATE# OR BORO?(3A) PHOSPHO?(3A)
                 SILICATE# OR (BOROPHOSPHO? OR PHOSPHOBORO?)(2A) SILICATE#
                 OR BORO?(2A) PHOSPHOSILICATE# OR PHOSPHO?(2A) BOROSILICATE#
L33       314021 SEA BUBBL? OR CAVIT? OR MICROBUBBL? OR MICROCAVIT? OR
                 NANOBUBBL? OR NANOCAVIT?
L34       473898 SEA BUBBL? OR CAVIT? OR MICROBUBBL? OR MICROCAVIT? OR
                 NANOBUBBL? OR NANOCAVIT?
L35       120416 SEA BUBBL? OR CAVIT? OR MICROBUBBL? OR MICROCAVIT? OR
                 NANOBUBBL? OR NANOCAVIT?
     TOTAL FOR ALL FILES
L36       908335 SEA BUBBL? OR CAVIT? OR MICROBUBBL? OR MICROCAVIT? OR
                 NANOBUBBL? OR NANOCAVIT?
L37          890 SEA L1 AND (L17 OR L21) AND (L25 OR L29)
L38         1039 SEA L2 AND (L18 OR L22) AND (L26 OR L30)
L39          169 SEA L3 AND (L19 OR L23) AND (L27 OR L31)
     TOTAL FOR ALL FILES
L40         2098 SEA L4 AND (L20 OR L24) AND (L28 OR L32)
L41           12 SEA L37 AND L33
L42           24 SEA L38 AND L34
L43            2 SEA L39 AND L35
     TOTAL FOR ALL FILES
L44           38 SEA L40 AND L36
L45            1 SEA L41 AND (L9 OR L13)
L46            2 SEA L42 AND (L10 OR L14)
L47            0 SEA L43 AND (L11 OR L15)
     TOTAL FOR ALL FILES
L48            3 SEA L44 AND (L12 OR L16)
L49            0 SEA L41 AND L5
L50            0 SEA L42 AND L6
L51            0 SEA L43 AND L7
     TOTAL FOR ALL FILES
L52            0 SEA L44 AND L8
L53          132 SEA L1 AND L17 AND L25
L54           92 SEA L2 AND L18 AND L26
L55            5 SEA L3 AND L19 AND L27
     TOTAL FOR ALL FILES
L56          229 SEA L4 AND L20 AND L28
L57           19 SEA L53 AND (L9 OR L13)
L58            9 SEA L54 AND (L10 OR L14)
L59            0 SEA L55 AND (L11 OR L15)
     TOTAL FOR ALL FILES
L60           28 SEA L56 AND (L12 OR L16)
L61          890 SEA L1 AND (L17 OR L21) AND (L25 OR L29)
L62         1039 SEA L2 AND (L18 OR L22) AND (L26 OR L30)
L63          169 SEA L3 AND (L19 OR L23) AND (L27 OR L31)
     TOTAL FOR ALL FILES
L64         2098 SEA L4 AND (L20 OR L24) AND (L28 OR L32)
L65            5 SEA L61 AND L5
L66           22 SEA L62 AND L6
L67            0 SEA L63 AND L7
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     TOTAL FOR ALL FILES
L68          27 SEA L64 AND L8
L69           0 SEA L65 AND (L9 OR L13)
L70           0 SEA L66 AND (L10 OR L14)
L71           0 SEA L67 AND (L11 OR L15)
     TOTAL FOR ALL FILES
L72           0 SEA L68 AND (L12 OR L16)
L73          82 SEA L61 AND (L9 OR L13)
L74         106 SEA L62 AND (L10 OR L14)
L75          25 SEA L63 AND (L11 OR L15)
     TOTAL FOR ALL FILES
L76         213 SEA L64 AND (L12 OR L16)
L77           0 SEA L73 AND L5
L78           0 SEA L74 AND L6
L79           0 SEA L75 AND L7
     TOTAL FOR ALL FILES
L80           0 SEA L76 AND L8
L81           1 SEA L73 AND L33
L82           2 SEA L74 AND L34
L83           0 SEA L75 AND L35
     TOTAL FOR ALL FILES
L84           3 SEA L76 AND L36
L85           9 SEA L61 AND L13
L86          10 SEA L62 AND L14
L87           0 SEA L63 AND L15
     TOTAL FOR ALL FILES
L88          19 SEA L64 AND L16

     FILE 'HCA' ENTERED AT 16:56:01 ON 20 JAN 2011
L89         117 SEA BRUEL M?/AU
L90      108021 SEA PLATE#/TI
L91           1 SEA L89 AND L90

     FILE 'HCA, WPIX, JAPIO' ENTERED AT 17:07:22 ON 20 JAN 2011
L94      115925 SEA INTERLAYER? OR INTERFILM? OR INTERCOAT? OR (INTER OR
                INTERMEDIAT?)(2A)(LAYER? OR FILM? OR COAT?)
L95      103875 SEA INTERLAYER? OR INTERFILM? OR INTERCOAT? OR (INTER OR
                INTERMEDIAT?)(2A)(LAYER? OR FILM? OR COAT?)
L96       53483 SEA INTERLAYER? OR INTERFILM? OR INTERCOAT? OR (INTER OR
                INTERMEDIAT?)(2A)(LAYER? OR FILM? OR COAT?)
     TOTAL FOR ALL FILES
L97      273283 SEA L93
L98         171 SEA L1 AND (L17 OR L21) AND (L25 OR L29) AND L94
L99         209 SEA L2 AND (L18 OR L22) AND (L26 OR L30) AND L95
L100         57 SEA L3 AND (L19 OR L23) AND (L27 OR L31) AND L96
     TOTAL FOR ALL FILES
L101        437 SEA L4 AND (L20 OR L24) AND (L28 OR L32) AND L97
L102          1 SEA L98 AND L5
L103          0 SEA L99 AND L6
L104          0 SEA L100 AND L7
     TOTAL FOR ALL FILES
L105          1 SEA L101 AND L8
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L106          1 SEA L98 AND L13
L107          2 SEA L99 AND L14
L108          0 SEA L100 AND L15
     TOTAL FOR ALL FILES
L109          3 SEA L101 AND L16
L110          3 SEA L98 AND L33
L111          2 SEA L99 AND L34
L112          1 SEA L100 AND L35
     TOTAL FOR ALL FILES
L113          6 SEA L101 AND L36
L114          8 SEA L98 AND L25
L115         12 SEA L99 AND L26
L116          0 SEA L100 AND L27
     TOTAL FOR ALL FILES
L117         20 SEA L101 AND L28
L118        164 SEA L98 AND L29
L119        205 SEA L99 AND L30
L120         57 SEA L100 AND L31
     TOTAL FOR ALL FILES
L121        426 SEA L101 AND L32
L122          1 SEA L114 AND L118
L123          8 SEA L115 AND L119
L124          0 SEA L116 AND L120
     TOTAL FOR ALL FILES
L125          9 SEA L117 AND L121

     FILE 'JAPIO' ENTERED AT 18:47:03 ON 20 JAN 2011
L126          7 SEA L43 OR L55 OR L112

     FILE 'WPIX' ENTERED AT 18:47:28 ON 20 JAN 2011
L127         29 SEA L46 OR L58 OR L82 OR L86 OR L107 OR L111 OR L123
L128         46 SEA (L42 OR L66 OR L115) NOT L127

     FILE 'HCA' ENTERED AT 18:48:34 ON 20 JAN 2011
L129         26 SEA L45 OR L65 OR L81 OR L85 OR L102 OR L106 OR L110 OR
                L114 OR L122
L130         21 SEA (L41 OR L57) NOT L129
L131         16 SEA 1802-2003/PY,PRY,AY AND L129
L132         17 SEA 1802-2003/PY,PRY,AY AND L130

     FILE 'WPIX' ENTERED AT 18:51:14 ON 20 JAN 2011
L133         19 SEA 1802-2003/PY,PRY,AY AND L127
L134         36 SEA 1802-2003/PY,PRY,AY AND L128

     FILE 'JAPIO' ENTERED AT 18:52:07 ON 20 JAN 2011
L135          7 SEA 1802-2003/PY,PRY,AY AND L126
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=> FILE JAPIO
FILE 'JAPIO' ENTERED AT 18:53:12 ON 20 JAN 2011
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FILE LAST UPDATED:            10 JAN 2011       <20110110/UP>
MOST RECENT PUBLICATION DATE: 30 SEP 2010       <20100930/PD>


=> D L126 1-7 BIB ABS IND

L126 ANSWER 1 OF 7  JAPIO  (C) 2011 JPO  on STN
AN    2000-058542    JAPIO  Full-text
TI    FORMATION OF DIELECTRIC MATERIAL ON SILICON MATERIAL, METHOD FOR
      REDUCING CAPACITANCE FORMED ON SILICON SUBSTRATE,
      AND DRAM CELL HAVING CAPACITIVELY COUPLED TRANSISTOR
IN    SCHREMS MARTIN; VOLLERTSEN ROLF-PETER; HOEPFNER JOACHIM
PA    SIEMENS AG
PI    JP 2000058542 A  20000225 Heisei
AI    JP 1999-182256 (JP11182256 Heisei) 19990628
PRAI  US 1998-105633      19980626
SO    PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AN    2000-058542    JAPIO  Full-text
AB     PROBLEM TO BE SOLVED: To provide a method by which a low-capacitance
       dielectric insulating film can be formed by forming a silicon dioxide
       dielectric layer on the surface of silicon, and reducing the permittivity
       between the silicon and silicon dioxide by treating the surface of the
       silicon with hydrogen. SOLUTION: A silicon dioxide layer 11 is formed on the
       upper surface of a semiconductor body 10 almost by thermal oxidation by
       using silicon containing a p-type conductivity boron dopant. The part of the
       silicon dioxide layer 11 exposed through an aperture 17 is removed, and a
       silicon dioxide dielectric layer 16 is thermally grown on the silicon body
       10 by rapid thermal oxidation. Then the dielectric layer 16 is baked with a
       hydrogen gas in a hydrogen- containing furnace. A naturally existing
       residual sacrificial silicon oxide layer is removed in advance and, even
       when the hydrogen passivation area 14 is formed before or after the
       formation of the silicon oxide layer 16, the upper surface layer 14 of the
       hydrogen passivation area 14 or silicon body 10 is formed.
       COPYRIGHT: (C)2000,JPO
IC    ICM  H01L021-316
      ICS  H01L021-762; H01L027-04; H01L021-822; H01L027-108; H01L021-8242

L126 ANSWER 2 OF 7  JAPIO  (C) 2011 JPO  on STN
AN    1998-150111    JAPIO  Full-text
TI    MANUFACTURE OF MIS TRANSISTOR
IN    HASEBE YUJI
PA    DENSO CORP
PI    JP 10150111 A  19980602 Heisei
AI    JP 1996-305080 (JP08305080 Heisei) 19961115
PRAI  JP 1996-305080      19961115
SO    PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998
AN    1998-150111    JAPIO  Full-text
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AB PROBLEM TO BE SOLVED: To manufacture an MIS transistor of salicide structure having excellent leak current characteristics in a source and a drain even when gate length becomes short. SOLUTION: An N-well layer 2 and a P-wall layer 3 are formed on single crystal P-type silicon substrate 1, and a gate electrode 6 is formed on the N-well layer 2 and the P-well layer 3. After phosphorus and boron-doped silicon oxide films 9 and 10 have been formed, the phosphorus and boron are subjected to solid phase diffusion into the well layers 2 and 3 by conducting heat treatment, and a source and drain 11 is formed. Besides, a titanium film is formed, the titanium film is subjected to salicide reaction, and a titanium-silicide film is epitaxially grown. As the source and drain 11 is formed by solid phase diffusion as above-mentioned, crystal lattice is not almost destructed, and as a single crystal substrate is used, the direction, etc., of the epitaxial growth of the titanium/silicide film can be constantly maintained, and the generation of spikes can be prevented, and the generation of a leak current can also be prevented. COPYRIGHT: (C)1998,JPO

IC ICM H01L021-8238
ICS H01L027-092; H01L021-28; H01L029-78

L126 ANSWER 3 OF 7 JAPIO (C) 2011 JPO on STN
AN 1989-205550 JAPIO Full-text
TI MANUFACTURE OF SEMICONDUCTOR ELEMENT
IN HONMA NOBUYUKI; MATSUI HIROSHI
PA OKI ELECTRIC IND CO LTD
PI JP 01205550 A 19890817 Heisei
AI JP 1988-28884 (JP63028884 Showa) 19880212
PRAI JP 1988-28884 19880212
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1989
AN 1989-205550 JAPIO Full-text
AB PURPOSE: To prevent the shape of the surface from being changed, to prevent a protrusion from being formed and to eliminate an unetched part by separating a boron-phosphorus doped silicon oxide film from a conductive layer by using a silicon oxide film having no reflow effect. CONSTITUTION: An insulating film 2 is formed on a silicon substrate 1; a first- layer wiring part 3 is formed on it. After a boronphosphorus doped silicon oxide film 4 has been formed, the oxide film 4 is heat-treated. A high melting-point film, e.g., a silicon oxide film 7, is formed on the oxide film 4. A conductive layer to be used as a second-layer wiring part, e.g., a polycrystalline silicon layer 5, is formed on the silicon oxide film 7. Phosphorus is diffused in the whole surface of the silicon layer 5. By this setup, it is possible to prevent the shape of the surface from being changed, to prevent a protrusion from being formed and to eliminate an unetched part. COPYRIGHT: (C)1989,JPO&Japio

IC ICM H01L021-90
ICS H01L021-95

L126 ANSWER 4 OF 7 JAPIO (C) 2011 JPO on STN
AN 1988-308350 JAPIO Full-text
TI FORMATION OF INSULATING LAYER
IN FURUMURA YUJI; UOOCHI YASUO
PA FUJITSU LTD
PI JP 63308350 A 19881215 Showa

AI   JP 1987-144273 (JP62144273 Showa) 19870610
PRAI JP 1987-144273   19870610
SO   PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1988
AN   1988-308350   JAPIO Full-text
AB   PURPOSE: To prevent the occurrence of voids due to air bubbles trapped in an insulating layer in the fine gaps between wirings by performing a heat treatment (reflow process) for planarizing the surface of the interlayer insulating layer in a high-pressure helium atmosphere.

CONSTITUTION: To a high-pressure vessel 1 made of stainless steel, a gas introducing pipe 2 and a gas exhaust pipe 3 are connected respectively through a cut-off valve 4 and a pressure regulator valve 5, and a semiconductor substrate 6 received in a holder 7 is placed in the center of the high-pressure vessel 1. On the surface of the semiconductor substrate 6, a film to be subjected to a planarization heat treatment is formed which is made of phosphosilicate glass or the like, and around the holder 7, a heater 8 is provided for heating the semiconductor substrate 6. And the glass layer of the phosohosilicate or borophosphosilicate system produced on the semiconductor chip surface having a plurality of wirings arranged at fine intervals is heated in a high-pressure atmosphere so as to reflow. With this, the occurrence of voids in the insulating layer consisting of the phosphosilicate or borophosphosilicate system glass layer in the gaps between the wirings is prevented. COPYRIGHT: (C)1988,JPO&Japio
IC   ICM H01L021-90
     ICS H01L021-316

L126 ANSWER 5 OF 7 JAPIO (C) 2011 JPO on STN
AN   1986-264736   JAPIO Full-text
TI   MANUFACTURE OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
IN   TAKEMURA HISASHI
PA   NEC CORP
PI   JP 61264736 A 19861122 Showa
AI   JP 1985-105520 (JP60105520 Showa) 19850517
PRAI JP 1985-105520   19850517
SO   PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1986
AN   1986-264736   JAPIO Full-text
AB   PURPOSE: To eliminate a cavity or grooves on the surface having an adverse effect on the formation of elements by forming the deep first groove in the first hole formed on a semiconductor substrate when forming a separating groove of different depth on the substrate, then etching the substrate exposed with the second hole, and a polycrystalline silicon film coated in advance and exposed with the first hole, forming the two shallow second grooves, allowing the coated insulating film to remain in the shallow groove, and removing the other.

CONSTITUTION: After a hole is formed on a silicon oxide film 102 by a photoetching method, the deep first groove 103 is selectively formed. The surface of the first groove 103 is oxidized, a phosphorus-doped polycrystalline silicon film 105 is accumulated, and the first groove 103 is buried. A silicon semiconductor substrate 101 and the film 105 are simultaneously etched by an anisotropic etching method to form the two shallow second grooves 107, 108. The surface of the substrate 101 is exposed, oxidized together with the surface of the film 105, a boron

phosphosilicate glass film 110 is then accumulated, allowed to reflow to flatten the surface, then etched to expose a silicon oxide film 109.

IC ICM H01L021-76

L126 ANSWER 6 OF 7 JAPIO (C) 2011 JPO on STN
AN 1984-218777 JAPIO Full-text
TI SEMICONDUCTOR DEVICE
IN KAKIZAKI KATSUNOBU; FUJIMOTO YOSHIHARU
PA NEC CORP
PI JP 59218777 A 19841210 Showa
AI JP 1984-90687 (JP59090687 Showa) 19840507
PRAI JP 1984-90687 19840507
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1984
AN 1984-218777 JAPIO Full-text
AB PURPOSE: To obtain a semiconductor device which has an N type conductive region including less lattice defect and small junction leakage current by doping arsenic together with boron on a P type silicon substrate,and providing a transistor having source and drain regions doped with the phosphorus. CONSTITUTION: A silicon dioxide film 2 is formed on the surface of a P type silicon substrate 1 doped with arsenic and boron. Silicon dioxide film to become source and drain are then selectively removed, phosphorus is diffused, and oxidation pressing is executed in oxidative atmosphere to form a source region 3 and a drain region 4. Then, silicon dioxide film of the region 5 to become a gate between the region 3 and the region 4 is selectively removed. Thereafter, it is thermally oxidized to grown a gate oxidized film 6. Subsequently, a gate electrode 7, a source electrode 8, and a drain electrode 9 are formed.

IC ICM H01L029-78

L126 ANSWER 7 OF 7 JAPIO (C) 2011 JPO on STN
AN 1979-064985 JAPIO Full-text
TI MANUFACTURE OF SEMICONDUCTOR DEVICE
IN FUKUCHI JUN; YOSHIDA MANABU
PA MATSUSHITA ELECTRIC IND CO LTD
PI JP 54064985 A 19790525 Showa
AI JP 1977-131714 (JP52131714 Showa) 19771101
PRAI JP 1977-131714 19771101
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1979
AN 1979-064985 JAPIO Full-text
AB PURPOSE: To obtin a solar battery element featuring a high photoelectric conversion efficiency by coating the silica film containing the P-type and N-type impurities onto the both surfaces of the semiconductor substrate and giving a heat treatment in the dried N<SB>2</SB> gas containing 5∼7% HCl at 1000∼1200°C. CONSTITUTION: The silica doped with P or As is rotary-applied to the surface of N-type Si substrate 1, and the solvent is evaporated with a heat treatment at about 200°C to form silica films 8 and 8' on the surface and at the side of the substrate with about 300Å thickness. In the similar way, non-doped silica film gand 9' to be used as the mask are coated to about 3500Å thickness, nd about 4000Å B-doped silica film 10 is formed on the back, with film 9' and 8' removed at

the side. After this, a heat treatment is given in the dried N<SB>2</SB> gas containing 5∼7% HCl and at 1000∼1200°C to diffuse the impurities in the film. Thus, N<SP>+</SP>-type layer 4 and P<SP>+</SP>- type layer 2 are caused under film 8 and 10 respectively. Then film 8 and 9 are removed, and layer 2 is covered with SiO<SB>2</SB> film 3, and electrode 6 is provided via an opening. At the same time, electrode 5 is attached on layer 4 as well. COPYRIGHT: (C)1979,JPO&Japio

IC ICM H01L031-04

=> FILE HCA

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=> D L131 1-16 BIB ABS HITIND

L131 ANSWER 1 OF 16 HCA COPYRIGHT 2011 ACS on STN

AN 142:488193 HCA Full-text

TI Silicon-based porous substrates, their production, and their use as filters, for chromatography, and in the synthesis of molecules such as oligonucleotides

IN Lehmann, Volker; Fuchs, Karin; Haneder, Thomas; Fritz, Michaela

PA Infineon Technologies Ag, Germany

SO Ger. Offen., 7 pp.
CODEN: GWXXBX

DT Patent

LA German

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 10348541	A1	20050519	DE 2003-10348541	20031020
PRAI	DE 2003-10348541		20031020		

AB Silicon-based porous substrates comprising a porous primary structure formed from macropores which are essentially parallel and which extend from the upper to the lower surface of the substrate are described which are provided with a porous secondary structure consisting of mesopores formed at least in selected regions of the sidewalls of the macropores. The substrates may be provided, at least in some sections, with surface layers formed from SiO2, Si3N4, or a silane. Methods for the prodn. of the substrates are described which entail providing an n-doped monocryst. Si substrate, generating macropores using electrochem. etching, doping the substrate using a borosilicate or phosphosilicate glass dopant source, and generating mesopores using electrochem. etching. Use of the substrates as filters, for chromatog., and in the synthesis of mols., in particular biomols. such as oligonucleotides, is also described.

CC   66-6 (Surface Chemistry and Colloids)
     Section cross-reference(s): 9
ST   silicon porous substrate prodn; filter
     silicon porous substrate; chromatog silicon
     porous substrate; oligonucleotide synthesis silicon
     porous substrate
IT   Borosilicate glasses
       Phosphosilicate glasses
        (in silicon-based porous substrate prodn.)
IT   Filters
        (silicon-based porous substrates and their
        prodn. and their use as)
IT   Porous materials
        (silicon-based porous substrates and their
        prodn. and their use as filters and for chromatog. and in mol.
        synthesis)
IT   Silanes
        (silicon-based porous substrates and their
        prodn. and their use as filters and for chromatog. and in mol.
        synthesis)
IT   Chromatographic stationary phases
        (silicon-based porous substrates and their
        prodn. and their use in)
IT   Biochemical compounds
        (silicon-based porous substrates and their
        prodn. and their use in synthesis of)
IT   Oligonucleotides
        (silicon-based porous substrates and their
        prodn. and their use in the synthesis of)
IT   7440-21-3, Silicon, processes
        (silicon-based porous substrates and their
        prodn. and their use as filters and for chromatog. and in mol.
        synthesis)
IT   7631-86-9, Silica, uses   12033-89-5, Silicon nitride, uses
        (silicon-based porous substrates and their
        prodn. and their use as filters and for chromatog. and in mol.
        synthesis)
OSC.G   1   THERE ARE 1 CAPLUS RECORDS THAT CITE THIS RECORD (1 CITINGS)
RE.CNT 3   THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
              ALL CITATIONS AVAILABLE IN THE RE FORMAT

L131 ANSWER 2 OF 16 HCA COPYRIGHT 2011 ACS on STN
AN   142:327633 HCA Full-text
TI   Process for fabricating a plate-shaped silicon
     structure, application of the process, and plate-shaped
     silicon structure
IN   Bruel, Michel
PA   Bruel Michel, Fr.
SO   Fr. Demande, 24 pp.
     CODEN: FRXXBL
DT   Patent
LA   French

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	FR 2860249	A1	20050401	FR 2003-11450	20030930
	FR 2860249	B1	20051209		
	WO 2005034218	A2	20050414	WO 2004-FR2398	20040923
	WO 2005034218	A3	20050728		
	EP 1671361	A2	20060621	EP 2004-787425	20040923
	EP 1671361	B1	20070404		
	CN 1883031	A	20061220	CN 2004-80033848	20040923
	CN 100514560	C	20090715		
	JP 2007507872	T	20070329	JP 2006-530396	20040923
	AT 358889	T	20070415	AT 2004-787425	20040923
	KR 2006117925	A	20061117	KR 2006-7008261	20060428
	US 20080038564	A1	20080214	US 2007-574120	20070531
PRAI	FR 2003-11450	A	20030930		
	WO 2004-FR2398	W	20040923		

ASSIGNMENT HISTORY FOR US PATENT AVAILABLE IN LSUS DISPLAY FORMAT

AB A manufg. process is described of a structure in form of plate, and structure in the shape of plate, in particular out of silicon, comprising at least a substrate, a superstratum and at least an intermediate layer interposed between the substrate and the superstratum, in which the intermediate layer comprises at least a basic material in which are distributed atoms or mols. known as extrinsic, different from the atoms or mols. from basic material, and in which one applies a heat treatment to the aforementioned plate such as, in the range of temp. of this heat treatment, the intermediate layer is plastically deformable and the presence of the atoms or mols. extrinsic chosen in the basic material engenders in an irreversible way the formation of microbubbles or microcavities in the intermediate layer.

IPCI C30B0033-02 [ICM,7]; C30B0033-00 [ICM,7,C*]; H01L0021-20 [ICS,7]; H01L0021-322 [ICS,7]; H01L0021-02 [ICS,7,C*]; H01L0021-762 [ICS,7]; H01L0021-70 [ICS,7,C*]

IPCR C30B0033-00 [I,C*]; C30B0033-00 [I,A]; C30B0033-02 [I,A]; H01L0021-02 [I,C*]; H01L0021-20 [I,A]; H01L0021-70 [I,C*]; H01L0021-762 [I,A]

CC 76-3 (Electric Phenomena)

ST process fabricating plate shaped silicon structure

IT Bubbles
(microbubbles; process for fabricating plate -shaped silicon structure, application of process, and plate-shaped silicon structure)

IT Heat treatment
Interfacial structure
(process for fabricating plate-shaped silicon structure, application of process, and plate-shaped silicon structure)

IT Borophosphosilicate glasses
Phosphosilicate glasses
(process for fabricating plate-shaped silicon structure, application of process, and plate-shaped silicon structure)

IT 7723-14-0, Phosphorus, processes
(process for fabricating plate-shaped silicon

structure, application of process, and plate-shaped
silicon structure)
IT 7440-21-3, Silicon, processes 7631-86-9, Silica, processes
(process for fabricating plate-shaped silicon
structure, application of process, and plate-shaped
silicon structure)
OSC.G 4 THERE ARE 4 CAPLUS RECORDS THAT CITE THIS RECORD (4 CITINGS)
RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L131 ANSWER 3 OF 16 HCA COPYRIGHT 2011 ACS on STN
AN 141:234340 HCA Full-text
TI Fabrication of semiconductor devices by forming an interlayer
insulator film without burying defects
IN Kosugi, Takeshi
PA Renesas Technology Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2004247369	A	20040902	JP 2003-33138	20030212
PRAI	JP 2003-33138		20030212		

AB The tile fabrication involves (1) patterning gate contacts on patterned gate insulator thin films on a semiconductor substrate, (2) depositing a B/P- doped 1st silica thick film by 1st CVD over the gate contacts on the substrate, (3) reflowing the 1st silica thick film, and (4) depositing a 2nd silica thick film over the 1st silica thick film by 2nd CVD with O2 concn. higher and the deposition temp. higher than those in the 1st CVD to give a 1st/2nd composite silica interlayer insulator film. The process providing the double-layer interlayer insulator film prevents insufficient burying of insulator film and consequent depletion region formation. IPCI H01L0029-78 [ICM,7]; H01L0029-66 [ICM,7,C*]; H01L0021-316 [ICS,7];
H01L0021-02 [ICS,7,C*]
IPCR H01L0021-02 [I,C*]; H01L0021-316 [I,A]; H01L0029-66 [I,C*];
H01L0029-78 [I,A]
CC 76-3 (Electric Phenomena)
IT Semiconductor device fabrication
(fabrication of semiconductor devices by forming an
interlayer insulator film without burying defects)
IT Electric double layer
(interlayer insulator film; fabrication of semiconductor
devices by forming an interlayer insulator film without
burying defects)
IT Dielectric films
(interlayer, CVD burying gate contacts; fabrication of
semiconductor devices by forming an interlayer insulator
film without burying defects)
IT Vapor deposition process
(of composite silica insulator film; fabrication of semiconductor

devices by forming an interlayer insulator film without
burying defects)

IT Annealing
(reflowing of insulator films; fabrication of semiconductor devices by forming an interlayer insulator film without burying defects)

IT 7631-86-9, Silica, properties
(interlayer insulator film, composite; fabrication of semiconductor devices by forming an interlayer insulator film without burying defects)

L131 ANSWER 4 OF 16 HCA COPYRIGHT 2011 ACS on STN

AN 141:31647 HCA Full-text

TI Sealing of cavities with lateral feed-throughs by anodic bonding

AU Fleron, R. W.; Jensen, F.

CS Mikroelektronik Centret, Technical University of Denmark, Lyngby, DK-2800, Den.

SO Proceedings - Electrochemical Society (2003), 2003-19, 337-345
CODEN: PESODO; ISSN: 0161-6374

PB Electrochemical Society

DT Journal

LA English

AB The SESiBon project under the EU Growth program has focussed on the investigation and exploitation of various silicon bonding techniques. Both std. silicon to pyrex wafer bonding and the more advanced silicon-to-silicon thin film anodic bonding has been investigated. Here we present the results of the work done to enable bonding of structured wafer surfaces, allowing lateral feed-throughs into sealed cavities. Lateral feed throughs are formed by means of RIE in a high-doped poly-silicon film deposited on an oxidized 4'' silicon wafer. Next a BPSG (Boron Phosphorus Silicate Glass) layer is deposited in a PECVD reaction chamber onto the structured surface. The BPSG is used as an intermediate planarization layer. Planarization is done by annealing the wafer in a N2-O2-H2O ambient for 4-8 h @ 900°. After planarization the two wafers are bonded together, sealing the cavities. Our work with BPSG has proven that although it is not trivial, planarization of structured wafer surfaces to a flatness necessary for bonding is feasible. It is necessary to design the lateral feed-through structures in accordance with the BPSG floating properties allowing space for the glass to flow into the valleys of the surface.

CC 76-2 (Electric Phenomena)

ST cavity sealing semiconductor wafer anodic bonding

IT Water vapor
(annealing process gas; sealing of cavities with lateral feed-throughs by anodic bonding)

IT Joining
(anodic bonding; sealing of cavities with lateral feed-throughs by anodic bonding)

IT Annealing
(planarization aided by; sealing of cavities with lateral

feed-throughs by anodic bonding)
IT Polishing
(sealing of cavities with lateral feed-throughs by anodic bonding)
IT Borophosphosilicate glasses
(sealing of cavities with lateral feed-throughs by anodic bonding)
IT 7727-37-9, Nitrogen, processes 7782-44-7, Oxygen, processes
(annealing process gas; sealing of cavities with lateral feed-throughs by anodic bonding)
IT 7440-21-3, Silicon, properties
(sealing of cavities with lateral feed-throughs by anodic bonding)
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L131 ANSWER 5 OF 16 HCA COPYRIGHT 2011 ACS on STN
AN 140:397212 HCA Full-text
TI Integrated optical circuit with dense planarized cladding layer
IN Gill, David M.; King, Oliver S.; Johnson, Frederick G.
PA USA
SO U.S. Pat. Appl. Publ., 13 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 20040087049	A1	20040506	US 2003-441052	20030520
	US 20040201026	A1	20041014	US 2004-837685	20040504
	US 6949392	B2	20050927		
PRAI	US 2002-423162P	P	20021104		
	US 2003-441052	A3	20030520		

ASSIGNMENT HISTORY FOR US PATENT AVAILABLE IN LSUS DISPLAY FORMAT
AB Integrated optical circuits are described which comprise a substrate; a first cladding layer having a first refractive index positioned on the substrate; a first core layer having a core refractive index including one or more defined waveguiding elements formed on the first cladding layer; a second cladding layer having a second cladding refractive index surrounding the waveguiding elements of the first core layer, the second cladding refractive index and the first cladding refractive index being less than the core refractive index, the second cladding layer being formed through simultaneous cladding material deposition and removal, the ratio of cladding material deposition to cladding material removal being ≈ > 1 and < 20 such that the second cladding layer is substantially void-free and substantially self-planarizing, enabling further layers to be directly positioned on the second cladding layer without necessitating intermediate planarization. Methods for forming the integrated optical circuits are also discussed.
CC 73-11 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)
Section cross-reference(s): 76

```
IT   Borosilicate glasses
       Phosphosilicate glasses
        (cladding; integrated optical circuit with dense planarized
        cladding layer)
IT   7631-86-9, Silica, uses
        (cladding, substrate; integrated optical circuit with
        dense planarized cladding layer)
IT   7440-42-8, Boron, uses   7440-44-0, Carbon, uses
     7440-56-4, Germanium, uses   7723-14-0, Phosphorus, uses
     14762-94-8, Fluorine, atomic, uses   17778-88-0, Nitrogen, atomic,
     uses
        (silica doped with; integrated optical circuit
        with dense planarized cladding layer)
IT   7440-21-3, Silicon, uses   60676-86-0, Vitreous
     silica
        (substrate; integrated optical circuit with dense
        planarized cladding layer)
OSC.G   1      THERE ARE 1 CAPLUS RECORDS THAT CITE THIS RECORD (1 CITINGS)
RE.CNT  20     THERE ARE 20 CITED REFERENCES AVAILABLE FOR THIS RECORD
               ALL CITATIONS AVAILABLE IN THE RE FORMAT

L131 ANSWER 6 OF 16  HCA  COPYRIGHT 2011 ACS on STN
AN   139:108475  HCA  Full-text
TI   Fabrication of optical waveguide structures with B- and/or
     P-doped silica glass core and claddings on
     silicon wafer substrates
IN   Temkin, Henryk; Kazarinov, Rudolf Feodor
PA   Applied WDM, Inc., USA
SO   U.S. Pat. Appl. Publ., 11 pp.
     CODEN: USXXCO
DT   Patent
LA   English
FAN.CNT 1
     PATENT NO.          KIND   DATE        APPLICATION NO.        DATE
     ---------------     ----   --------    --------------------   --------
PI   US 20030133682       A1    20030717    US 2002-47780          20020114
     US 6618537           B2    20030909
PRAI US 2002-47780              20020114
ASSIGNMENT HISTORY FOR US PATENT AVAILABLE IN LSUS DISPLAY FORMAT
AB    Solid state optical waveguide structures are fabricated comprising a boron
      and/or phosphorus doped silicon dioxide core layer sandwiched between lower
      and upper doped silicon dioxide cladding layers on a silicon semiconductor
      substrate.  The core and upper cladding layers are deposited using a plasma
      enhanced CVD process.  The core layer is patterned to define one or more
      waveguide cores.  The lower cladding layer is preferably also deposited
      using a plasma enhanced CVD process but alternatively may be formed by
      thermal oxidn.
CC   73-11 (Optical, Electron, and Mass Spectroscopy and Other Related
     Properties)
     Section cross-reference(s): 57, 76
ST   boron phosphorus dopant silica
     glass core cladding optical waveguide
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IT   Annealing
     Optical waveguides
     Refractive index
        (fabrication of optical waveguide structures with B-
        and/or P-doped silica glass core and
        claddings on silicon wafer substrates
)
IT   Vapor deposition process
        (plasma; fabrication of optical waveguide structures with B
        - and/or P-doped silica glass core
        and claddings on silicon wafer
        substrates)
IT   Semiconductor materials
        (substrates; fabrication of optical waveguide structures
        with B- and/or P-doped silica
        glass core and claddings on silicon wafer
        substrates)
IT   Oxidation
        (thermal; fabrication of optical waveguide structures with
        B- and/or P-doped silica
        glass core and claddings on silicon wafer
        substrates)
IT   1303-86-2, Boron oxide (B2O3), uses   1314-56-3,
     Phosphorus oxide (P2O5), uses   7440-42-8, Boron,
     uses   7723-14-0, Phosphorus, uses
        (dopant in silica glass; fabrication of optical
        waveguide structures with B- and/or P-
        doped silica glass core and claddings on
        silicon wafer substrates)
IT   60676-86-0P, Vitreous silica
        (doped, core and claddings; fabrication of optical waveguide
        structures with B- and/or P-doped
        silica glass core and claddings on silicon
        wafer substrates)
IT   7440-21-3, Silicon, uses
        (substrates; fabrication of optical waveguide structures
        with B- and/or P-doped silica
        glass core and claddings on silicon wafer
        substrates)
OSC.G   8   THERE ARE 8 CAPLUS RECORDS THAT CITE THIS RECORD (8 CITINGS)

L131 ANSWER 7 OF 16 HCA COPYRIGHT 2011 ACS on STN
AN   138:179196   HCA   Full-text
TI   Design and fabrication of a semiconductor device having a compliant
     substrate and a decoupling layer
IN   Demkov, Alexander A.
PA   Motorola, Inc., USA
SO   U.S. Pat. Appl. Publ., 29 pp.
     CODEN: USXXCO
DT   Patent
LA   English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
	---------------	----	--------	--------------------	--------
PI	US 20030038299	A1	20030227	US 2001-934836	20010823
PRAI	US 2001-934836		20010823		

ASSIGNMENT HISTORY FOR US PATENT AVAILABLE IN LSUS DISPLAY FORMAT

AB The invention relates to the design and fabrication of a semiconductor device having a compliant substrate and a decoupling layer. High quality epitaxial layers of monocryst. materials are grown overlying monocryst. substrates such as large silicon wafers by forming a compliant substrate for growing the monocryst. layers. The compliant substrate is formed by first growing an accommodating buffer layer on a silicon wafer. The accommodating buffer layer is a layer of monocryst. oxide spaced apart from the silicon wafer by an amorphous interface layer of silicon oxide. The amorphous interface layer dissipates strain and permits the growth of a high quality monocryst. oxide-accommodating buffer layer.

CC 76-3 (Electric Phenomena)
Section cross-reference(s): 57, 73, 75

ST semiconductor device compliant substrate
decoupling layer

IT Borophosphosilicate glasses
Borosilicate glasses
Phosphosilicate glasses
Silicate glasses
(amorphous oxide; design and fabrication of a semiconductor device having a compliant substrate and a decoupling layer)

L131 ANSWER 8 OF 16 HCA COPYRIGHT 2011 ACS on STN

AN 136:404297 HCA Full-text

TI Method for fabrication of solid oxide fuel cell including single cell with solid electrolyte

IN Kushibiki, Keiko; Sato, Fuminori; Hara, Naoki; Yamanaka, Mitsugu; Hatano, Masaharu; Uchiyama, Makoto; Shibata, Itaru; Fukuzawa, Tatsuhiro

PA Nissan Motor Co., Ltd., Japan

SO PCT Int. Appl., 135 pp.
CODEN: PIXXD2

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
	---------------	----	--------	--------------------	--------
PI	WO 2002043177	A2	20020530	WO 2001-JP10219	20011122
	WO 2002043177	A3	20030530		
	JP 2002222659	A	20020809	JP 2001-111102	20010410
	JP 3731648	B2	20060105		
	EP 1340281	A2	20030903	EP 2001-997862	20011122
	EP 1340281	B1	20100721		
	CN 1489799	A	20040414	CN 2001-805700	20011122
	CN 1271740	C	20060823		
	CN 1822422	A	20060823	CN 2006-10071505	20011122
	CN 100426581	C	20081015		
	EP 2144320	A2	20100113	EP 2009-13524	20011122

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     EP 2144320          A3    20100224
     US 20030012994      A1    20030116    US 2002-181258         20020716
     US 7122265          B2    20061017
     US 20070015033      A1    20070118    US 2006-523689         20060920
     US 7790328          B2    20100907
PRAI JP 2000-360353      A     20001127
     JP 2001-111102      A     20010410
     CN 2001-805700      A3    20011122
     EP 2001-997862      A3    20011122
     WO 2001-JP10219     W     20011122
     US 2002-181258      A3    20020716
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ASSIGNMENT HISTORY FOR US PATENT AVAILABLE IN LSUS DISPLAY FORMAT

AB In a single cell for a solid oxide fuel cell, a solid electrolyte layer is sandwiched by an upper electrode layer and a lower electrode layer. This single cell includes a substrate having openings and an insulating and stress absorbing layer stacked on an upper surface of this substrate. The solid electrolyte layer is formed on an upper surface of the insulating and stress absorbing layer so as to cover the openings, the upper electrode layer is stacked on an upper surface of the solid electrolyte layer, and the lower electrode layer is coated on a lower surface of the solid electrolyte layer via the openings from a lower surface of the substrate. In a cell plate, these single cells are disposed two-dimensionally on a common substrate. Furthermore, a solid oxide fuel cell, in which these cell plates and plate-shaped separators including gas passages on both surfaces thereof are alternately stacked.

CC 52-2 (Electrochemical, Radiational, and Thermal Energy Technology)

IT Phosphosilicate glasses
(insulating and stress-absorbing layer; method for fabrication of solid oxide fuel cell including single cell with solid electrolyte)

IT Borophosphosilicate glasses
(method for fabrication of solid oxide fuel cell including single cell with solid electrolyte)

IT 7440-21-3, Silicon, uses
(substrate; method for fabrication of solid oxide fuel cell including single cell with solid electrolyte)

OSC.G 8 THERE ARE 8 CAPLUS RECORDS THAT CITE THIS RECORD (12 CITINGS)

RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L131 ANSWER 9 OF 16 HCA COPYRIGHT 2011 ACS on STN

AN 132:101561 HCA Full-text

TI Semiconductor device with an aluminum fuse layer for memory application

IN Ido, Yasuhiro; Iwamoto, Takeshi; Toyota, Rui

PA Mitsubishi Denki K.K., Japan

SO Ger. Offen., 12 pp.
CODEN: GWXXBX

DT Patent

LA German

FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI	DE 19903208	A1	20000120	DE 1999-19903208	19990127
	DE 19903208	C2	20010517		
	JP 2000021990	A	20000121	JP 1998-190583	19980706
	JP 4397060	B2	20100113		
	US 6339250	B1	20020115	US 1998-213288	19981217
	TW 415037	B	20001211	TW 1999-101484	19990201
	KR 2000011188	A	20000225	KR 1999-7265	19990305
PRAI	JP 1998-190583	A	19980706		

ASSIGNMENT HISTORY FOR US PATENT AVAILABLE IN LSUS DISPLAY FORMAT

AB A semiconductor device structure with a protective aluminum layer is described for memory application. On a silicon substrate a silica layer is formed, on top of which is a layer of borophosphosilicate glass. Over the glass layer is a ≥ 1 μm protective silica layer doped with phosphorus. The metallic (Al) fuse layer is then sandwiched between this silica layer and another silica layer with no phosphorus. This top silica layer hinders corrosion of the metal layer, in order to provide the possibility of a semiconductor device with a highly dependable metallic connection.

CC 76-3 (Electric Phenomena)

IT Borophosphosilicate glasses
(layer of semiconductor device for memory applications)

OSC.G 2 THERE ARE 2 CAPLUS RECORDS THAT CITE THIS RECORD (2 CITINGS)

L131 ANSWER 10 OF 16 HCA COPYRIGHT 2011 ACS on STN

AN 127:12103 HCA Full-text

OREF 127:2340h,2341a

TI Fabricating a polysilicon electromigration sensor which can detect and monitor electromigration in composite metal lines on integrated circuit structures

IN Lin, Chih-sheng; Lee, Shun-yi

PA Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan

SO U.S., 11 pp.
CODEN: USXXAM

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5627101	A	19970506	US 1995-566808	19951204
	US 5846848	A	19981208	US 1997-796351	19970207
PRAI	US 1995-566808	A3	19951204		

ASSIGNMENT HISTORY FOR US PATENT AVAILABLE IN LSUS DISPLAY FORMAT

AB A polysilicon sensor is described which can be incorporated onto a Si wafer contg. integrated circuits for the purpose of detecting and monitoring electromigration (EM) in metal test stripes representative of the interconnection metallurgy used by the integrated circuits. The sensor capitalizes on the property of Si whereby a small increase in temp. causes a large increase in carrier concn. In this regard, the local temp. rise of an adjacent metal line undergoing EM failure manifests itself as a decrease in the resistance of the sensor. The sensor is particularly suited for testing multilevel metallurgies such as those having an Al alloy sandwiched between metallic layers such as those used for diffusion barriers and antireflective

coatings. Its fabrication is compatible with conventional MOSFET processes which use a self-aligned polysilicon gate. It can be particularly useful when built into the wafer kerf area or into a manufg. test site (MTS) where it can be used to test the quality of the metalization of a particular job. Structures built into the wafer kerf can be tested immediately after metalization, while those built into MTS chips can be reserved for long-term reliability testing.

CC 76-3 (Electric Phenomena)

IT Borophosphosilicate glasses
  Phosphosilicate glasses
   (fabricating a polysilicon electromigration sensor contg.)

OSC.G 5 THERE ARE 5 CAPLUS RECORDS THAT CITE THIS RECORD (5 CITINGS)

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L131 ANSWER 11 OF 16 HCA COPYRIGHT 2011 ACS on STN

AN 121:219388 HCA Full-text

OREF 121:39679a,39682a

TI Manufacture of semiconductor devices containing triple-layer insulator sidewalls for interconnection contacts

IN Maari, Koichi

PA Sony Corp., Japan

SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 06013342	A	19940121	JP 1992-167661	19920625
PRAI	JP 1992-167661		19920625		

AB The process includes: (a) successively forming 3 insulator films (e.g., borophosphosilicate, nitride, and phosphosilicate) on a Si substrate and gate electrodes; (b) etching the 3rd insulator film with the 2nd film as an etching stopper to form 3-layer sidewalls on the inside of the electrodes; (c) removing the 2nd insulator film in the contact area between the sidewalls; (d) removing the exposed 1st insulator film to expose the substrate, and (e) forming a metal interconnection. The 3-layer sidewalls do not cause current leaks between the gate electrodes and interconnection.

IPCI H01L0021-283 [ICM,5]; H01L0021-28 [ICS,5]; H01L0021-02 [ICS,5,C*]

IPCR H01L0021-28 [I,A]; H01L0021-02 [I,C*]; H01L0021-283 [I,A]

CC 76-3 (Electric Phenomena)

ST semiconductor device manuf multilayer insulator sidewall; phosphosilicate glass multilayer insulator sidewall; borophosphosilicate glass multilayer insulator sidewall; nitride multilayer insulator sidewall; interconnection semiconductor device

IT Electric contacts
  Electric insulators and Dielectrics
   (manuf. of semiconductor devices contg. triple-layer insulator sidewalls for interconnection contacts)

IT Nitrides

(manuf. of semiconductor devices contg. triple-
layer insulator sidewalls for interconnection contacts)

IT Semiconductor devices
(silicon; manuf. of semiconductor devices contg. triple-
layer insulator sidewalls for interconnection contacts)

IT 7440-21-3, Silicon, uses
(manuf. of semiconductor devices contg. triple-
layer insulator sidewalls for interconnection contacts)

L131 ANSWER 12 OF 16 HCA COPYRIGHT 2011 ACS on STN
AN 118:245815 HCA Full-text
OREF 118:42393a,42396a
TI Method for manufacture of insulated gate field effect transistor
IN Izawa, Tetsuo
PA Fujitsu Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04286127	A	19921012	JP 1991-50061	19910315
PRAI	JP 1991-50061		19910315		

AB The title method is composed of (1) formation of a gate insulating film on a semiconductor substrate, (2) lamination of a plural no. of semiconductor layers with a 1-3 nm thick insulating layer in between the semiconductor layer on the bottom semiconductor layer or formation of a multilayer gate electrode composed of semiconductor layers and metal layers, (3) introduction of a dopant to the semiconductor layer or metal layer except the bottom semiconductor layer to impart elec. cond. to the bottom semiconductor layer, and (4) heating the semiconductor substrate at ≥1050°to dissolve the interlayer insulating film of the multilayer gate electrode in the semiconductor or metal layer which makes contact with its upper and lower interlayer insulating films and at the same time to carry out solid-phase diffusion of the dopant from upper layer semiconductor or metal layer to the bottom layer semiconductor. The semiconductor substrate is Si and the semiconductor layers are polycryst. Si, the insulating layer is silicon oxide layer, and the dopant is B.

CC 76-3 (Electric Phenomena)

IT Transistors
(field-effect insulated-gate, boron ion doping in silicon
substrates in manuf. of)

IT Glass, oxide
(phosphosilicate, formation of, on silica
layers on silicon substrates in manuf. of
insulated gate field effect transistors)

IT 7440-42-8, Boron, miscellaneous
(doping of, in silicon substrate, for manuf. of
insulated gate field effect transistor)

IT 7631-86-9P, Silicon dioxide, preparation

(formation of, on silicon substrate followed by phosphosilicate glass formation in manuf. of insulated gate field effect transistors)

L131 ANSWER 13 OF 16 HCA COPYRIGHT 2011 ACS on STN
AN 118:31535 HCA Full-text
OREF 118:5589a,5592a
TI Manufacture of semiconductor device having interlayer insulator comprising impurity-containing top layer and impurity-free bottom layer
IN Kakiuchi, Koji
PA Seiko Instruments, Inc., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04236452	A	19920825	JP 1991-5246	19910121
PRAI	JP 1991-5246		19910121		

AB The title device has an interlayer elec. insulator comprising a bottom impurity-free Si oxide film and the top impurity-contg. Si oxide film. The device having the insulator, e.g., a laminated structure of an undoped Si oxide film and a B- and P-contg. Si oxide film, prevents the source and drain region from impurity migration in heating process.
CC 76-3 (Electric Phenomena)
ST silicon oxide impurity free insulator; boron phosphorus doped silica insulator
IT Semiconductor devices
(interlayer elec. insulator comprising bottom impurity-free silica film and top impurity-contg. silica film for)
IT Electric insulators and Dielectrics
(interlayer, impurity-free bottom silica film and impurity-contg. top silica film as, for semiconductor device)
IT 7440-42-8, Boron, uses 7723-14-0, Phosphorus, uses
(impurity, for interlayer elec. insulating silica film, impurity-free bottom layer for)
IT 11126-22-0, Silicon oxide
(interlayer elec. insulating film, impurity-free layer and impurity-contg. layer in)
IT 7440-21-3, Silicon, uses
(semiconductor substrate, interlayer elec. insulating silica film of impurity-free bottom layer and impurity-contg. top layer for)

L131 ANSWER 14 OF 16 HCA COPYRIGHT 2011 ACS on STN
AN 110:17314 HCA Full-text
OREF 110:2843a,2846a
TI Formation method for insulating interlayers of semiconductor devices
IN Kato, Hisayuki

PA   Hitachi, Ltd., Japan
SO   Jpn. Kokai Tokkyo Koho, 4 pp.
     CODEN: JKXXAF
DT   Patent
LA   Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 63182824	A	19880728	JP 1987-14026	19870126
PRAI	JP 1987-14026		19870126		

AB   A silanol or a silanol compd. is evapd. on a wafer in the vapor phase to form an insulating layer. The obtained SiO_2 insulating layer, useful as an interlayer of a semiconductor device, has decreased strain, as compared to a spin-on glass insulating layer, and is doped easily with P and B at a desired concn. IPCI H01L0021-316 [ICM,4]; H01L0021-02 [ICM,4,C*]
IPCR H01L0021-02 [I,C*]; H01L0021-316 [I,A]
CC   76-3 (Electric Phenomena)
ST   insulating interlayer semiconductor wafer
     ; silanol vapor evapn insulating interlayer
IT   Semiconductor devices
        (silanol vapor evapn. for insulating interlayer formation
        for)
IT   Electric insulators and Dielectrics
        (silica interlayer prepn. for, for semiconductor devices)
IT   7440-42-8, Boron, uses and miscellaneous   7723-14-0,
     Phosphorus, uses and miscellaneous
        (dopant, in silica insulating
        interlayer prepn. from silanol, for semiconductor device)
IT   7631-86-9, Silica, uses and miscellaneous
        (insulating interlayer of, by silanol vapor evapn., in
        semiconductor device prepn.)
IT   597-52-4   1066-40-6   14475-38-8   87963-93-7, Disilanol
        (silica insulating interlayer prepn. from, in vapor
        phase, in semiconductor device prepn.)

L131 ANSWER 15 OF 16 HCA COPYRIGHT 2011 ACS on STN
AN   105:235530 HCA Full-text
OREF 105:37889a,37892a
TI   Visible and ultraviolet semiconductor laser
IN   Blanchard, Bruno; Juliet, Pierre
PA   Commissariat a l'Energie Atomique, Fr.
SO   Fr. Demande, 16 pp.
     CODEN: FRXXBL
DT   Patent
LA   French
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	FR 2574602	A1	19860613	FR 1984-18902	19841211
PRAI	FR 1984-18902		19841211		

AB   A laser structure comprises several B- or P- doped SiO_2 layers juxtaposed alternatively with several layers of Si. The thickness of the Si layers are such

that they function as resonating cavities. The structure is excited by an elec. field. The elec. field is applied with 2 parallel electrodes placed on the 2 sides of the structure parallel to the SiO_2 and Si layer surfaces. The wavelength of the stimulated laser radiation is .ltorsim.100 nm.

IPCI H01S0003-18 [ICM,4]

IPCR H01L0033-00 [I,C*]; H01L0033-00 [I,A]; H01S0005-00 [I,C*]; H01S0005-04 [N,A]; H01S0005-10 [I,A]; H01S0005-30 [I,A]

CC 73-10 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)
Section cross-reference(s): 76

ST semiconductor laser silica silicon; silicon resonating cavity laser

RE.CNT 1 THERE ARE 1 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L131 ANSWER 16 OF 16 HCA COPYRIGHT 2011 ACS on STN

AN 79:36434 HCA Full-text

OREF 79:5895a,5898a

TI Semiconductor device

IN Nishimatsu, Shigeru; Tokuyama, Takashi

PA Hitachi, Ltd.

SO U.S., 5 pp.
CODEN: USXXAM

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 3730766	A	19730501	US 1969-864638	19691008
	JP 48013268	B	19730426	JP 1968-73133	19681009
PRAI	JP 1968-73133	A	19681009		

AB A triple-layer passivation film is used to control the amt. of induced elec. charge on the semiconductor substrate, in particular in a Si field-effect transistor. The 1st layer is electron inducing; the 2nd is hole inducing. Each layer is <1000 Å thick. The 3rd layer is electron inducing and of a thickness detd. by the amt. of charge to be induced on the substrate surface. The 1st and 3rd layers may be SiO_2, Si_3N_4, phosphosilicate glass, or borosilicate glass. The 2nd layer may be Al_2O_3, aluminosilicate glass, phosphoaluminosilicate glass, or SiO_2-diffused Zn. A SiO_2-Al_2O_3-SiO_2 structure is illustrated.

CC 71-13 (Electric Phenomena)

IT Transistors
(silicon field-effect, triple-layer passivation structure for channel inducement in)

IT 1344-28-1, uses and miscellaneous 7631-86-9, uses and miscellaneous
(coatings from triple layers contg., on silicon field-effect transistors, channel formation in relation to)

=> D L132 1-17 BIB ABS HITIND

L132 ANSWER 1 OF 17 HCA COPYRIGHT 2011 ACS on STN
AN 141:45902 HCA Full-text
TI Continuous platinum metal chemical vapor deposition with good step coverage
IN Derderian, Garo J.
PA Micron Technology, Inc., USA
SO U.S., 18 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6750110	B1	20040615	US 1998-121528	19980723
	US 20020000591	A1	20020103	US 1999-373355	19990812
	US 6861693	B2	20050301		
PRAI	US 1998-121528	A3	19980723		

ASSIGNMENT HISTORY FOR US PATENT AVAILABLE IN LSUS DISPLAY FORMAT
AB The invention relates generally to the chem. vapor deposition (CVD) of platinum group metals on an integrated circuit structure as a continuous film and with good step coverage. The invention also relates to integrated circuits having a platinum group metal layer, used, for example, as the lower electrode in a capacitor. A method is presented for depositing a Pt based metal film by CVD deposition includes bubbling a nonreactive gas over an org. Pt based metal precursor until the non-reactive gas is satd. with the precursor. The Pt based metal film is deposited onto a substrate in a CVD deposition chamber in the presence of both O2 and N2O at a predetd. temp. and under a predetd. pressure. The resulting film is consistently smooth and has good step coverage.
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 56, 75
IT Borophosphosilicate glasses
Oxides (inorganic), uses
Phosphosilicate glasses
Silicides
(substrate; continuous platinum metal chem. vapor deposition with good step coverage)
IT 7440-21-3, Silicon, uses 7440-32-6, Titanium, uses
12033-89-5, Silicon nitride, uses 25583-20-4, Titanium nitride (TiN)
(substrate; continuous platinum metal chem. vapor deposition with good step coverage)
OSC.G 1 THERE ARE 1 CAPLUS RECORDS THAT CITE THIS RECORD (1 CITINGS)
RE.CNT 13 THERE ARE 13 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L132 ANSWER 2 OF 17 HCA COPYRIGHT 2011 ACS on STN
AN 139:29381 HCA Full-text
TI Wafers, manufacturing wafers, and transfer masks using wafers thereof
IN Yotsui, Kenta; Gamo, Hidenori; Tamura, Akira
PA Toppan Printing Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.

CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2003174030	A	20030620	JP 2002-282574	20020927
PRAI	JP 2001-299774	A	20010928		

AB The title wafers have a single-cryst. Si substrate which is laminated with a SiO2 thin film. The SiO2 thin film is provided under stress-controlling and may preferably be doped with B, N, C, Ge, P, As, and/or Sb. The stress controlled SiO2 thin film on the substrates provides etching masks, etching stoppers, and transferring masks with increased degree of freedom. IPCI H01L0021-316 [ICM,7]; G03F0001-08 [ICS,7]; G03F0001-14 [ICS,7];
H01L0021-027 [ICS,7]; H01L0021-02 [ICS,7,C*]
IPCR G03F0001-08 [I,C*]; G03F0001-08 [I,A]; G03F0001-14 [I,C*]; G03F0001-14 [I,A]; H01L0021-02 [I,C*]; H01L0021-027 [I,A]; H01L0021-316 [I,A]
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 75
ST silicon wafer silica film
lamination stress control transfer mask
IT Stress, mechanical
(controlled, for silica thin film lamination; wafers and manufg. wafers and transfer masks using stress-controlled silica thin film on wafers)
IT Etching masks
(transferring; wafers and manufg. wafers and transfer masks using stress-controlled silica thin film on wafers)
IT Etch stops
Semiconductor materials
(wafers and manufg. wafers and transfer masks using stress-controlled silica thin film on wafers)
IT 7440-44-0P, Carbon, properties
(diamond-like, deposition on silicon substrate for transferring; wafers and manufg. wafers and transfer masks using stress-controlled silica thin film on wafers)
IT 7440-36-0, Antimony, uses 7440-38-2, Arsenic, uses 7440-42-8, Boron, uses 7440-56-4, Germanium, uses 7723-14-0, Phosphorus, uses 17778-88-0, Atomic nitrogen, uses
(dopant in silica thin film; wafers and manufg. wafers and transfer masks using stress-controlled silica thin film on wafers)
IT 7440-21-3, Silicon, properties
(single-crystal, substrate; wafers and manufg. wafers and transfer masks using stress-controlled silica thin film on wafers)
IT 7631-86-9, Silica, properties
(thin film, stress-controlled; wafers and manufg. wafers and transfer masks using stress-controlled silica thin film on wafers)

L132 ANSWER 3 OF 17 HCA COPYRIGHT 2011 ACS on STN
AN 138:162090 HCA Full-text
TI Semiconductor devices and fabrication of devices by deposition of polyimide films
IN Noritake, Chikage; Ino, Koji; Suzuki, Mikimasa
PA Denso Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2003045958	A	20030214	JP 2001-228282	20010727
PRAI	JP 2001-228282		20010727		

AB The title devices comprise a Si substrate, a 1st metal thin film formed on a portion of the insulated substrate, a polyimide thin film on the insulated substrate and overlapping over a peripheral portion of the 1st metal thin film, and a 2nd metal film on the 1st metal film and partially overlapping over a counter-peripheral portion of the polyimide film. The width of the 2nd metal overlapping on the peripheral portion of the polyimide film is ≤600 μm to make easy degassing out of the metal-overlapped polyimide in avoiding void formation and delamination of the polyimide film inside the laminate.
IPCI H01L0021-768 [ICM,7]; H01L0021-70 [ICM,7,C*]
IPCR H01L0021-70 [I,C*]; H01L0021-768 [I,A]; H01L0023-52 [I,C*]; H01L0023-522 [I,A]
CC 76-3 (Electric Phenomena)
IT Delamination
Voids (structures)
(prevention in polyimide insulator laminate; semiconductor devices and fabrication of devices by deposition of polyimide films)
IT 7440-42-8, Boron, uses 7723-14-0, Phosphorus, uses
(dopant in silica; semiconductor devices and fabrication of devices by deposition of polyimide films)

L132 ANSWER 4 OF 17 HCA COPYRIGHT 2011 ACS on STN
AN 137:162341 HCA Full-text
TI Microfabricated device structures with trench isolation using bonded substrates and cavities for integrated-circuit fabrication
IN Clark, William A.; Lemkin, Mark A.; Juneau, Thor N.; Roessig, Allen W.
PA Analog Devices IMI, Inc., USA
SO U.S., 21 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6433401	B1	20020813	US 2000-543936	20000405

PRAI US 1999-127973P P 19990406

ASSIGNMENT HISTORY FOR US PATENT AVAILABLE IN LSUS DISPLAY FORMAT

AB A microstructure and method for forming the microstructure are disclosed where the structural elements are formed by a high aspect-ratio process, MEMS fabrication has little effect on the substrate circuitry, and the structural elements are isolated where desired. The method includes: providing a handle substrate; providing a device substrate in which high-aspect-ratio structures and optional integrated circuitry will be fabricated; forming one or more filled isolation trenches within a recessed cavity on a 1st surface of the device substrate or alternatively forming one or more filled isolation trenches on a 1st surface of the device substrate and forming a recessed cavity on a 1st surface of the handle substrate; bonding the 1st surface of the device substrate to the 1st surface of the handle substrate; removing a substantially uniform amt. of material from the 2nd surface of the device substrate to expose at least one isolation trench; optionally forming circuits and interconnection on a 2nd surface of the device substrate; and etching a set of features in the 2nd surface of the device substrate to complete the definition of elec. isolated structural elements. The micromech. device includes: a device substrate having a 1st surface, a 2nd surface, and a semiconductor layer; a handle substrate, the 1st surface of the device substrate bonded to the handle substrate; one or more 1st trenches formed in the device substrate, the 1st trenches extending from the 2nd surface of the device substrate through the device substrate towards the handle substrate; a dielec. within the 1st trenches; one or more cavities disposed below the 2nd surface of the device layer, a cavity enclosing a portion of at least one trench; at least one 2nd trench formed in the 2nd surface of the device substrate, the 2nd trench completing definition of one or more micromech. devices.

CC 76-3 (Electric Phenomena)

IT Dielectric films
Electronic device fabrication
Etching
Integrated circuits
Interconnections, electric
Joining
Micromachines
SOI devices
Transistors
(microfabricated device structures with trench isolation using bonded substrates and cavities for integrated-circuit fabrication)

IT Arsenide glasses
Borate glasses
Borophosphosilicate glasses
Phosphosilicate glasses
(microfabricated device structures with trench isolation using bonded substrates and cavities for integrated-circuit fabrication)

IT 1344-28-1, Aluminum oxide, uses 7440-21-3, Silicon, uses
7631-86-9, Silicon dioxide, uses 12033-89-5, Silicon nitride, uses
(microfabricated device structures with trench isolation using bonded substrates and cavities for integrated-circuit

fabrication)
OSC.G 15 THERE ARE 15 CAPLUS RECORDS THAT CITE THIS RECORD (15 CITINGS)
RE.CNT 58 THERE ARE 58 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L132 ANSWER 5 OF 17 HCA COPYRIGHT 2011 ACS on STN
AN 135:365364 HCA Full-text
TI Thin-film transistors having polycrystal silicon on glass substrates and fabrication of transistors thereof
IN Ishiu, Takehiko
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001320057	A	20011116	JP 2000-138447	20000511
PRAI	JP 2000-138447		20000511		

AB The title TFTs comprise an insulative substrate, a reflowing polymer film for leveling over the insulative substrate, a diffusion barrier coating layer over the polymer leveling film, and a polycryst. Si semiconductor layer formed on the diffusion barrier layer for formation of source/drain regions provided across a channel region. The polymer leveling film is annealed to become a SiO_2 film contg. P, B, or the both dopants. The diffusion barrier may be a SiNx/SiO_2 multilayer. The use of the polymer leveling film over the glass substrates effectively eliminates device defects caused by its surface defects and voids for significant improvement of circuit patterns and components and consequent manufg. yields.
CC 76-3 (Electric Phenomena)
IT Diffusion barrier
(coating of; thin-film transistors having polycrystal silicon on glass substrates and fabrication of transistors thereof)
IT Surface defects
Voids (structures)
(elimination, by surface leveling; thin-film transistors having polycrystal silicon on glass substrates and fabrication of transistors thereof)
IT Annealing
(for reflowing and sintering of polymer; thin-film transistors having polycrystal silicon on glass substrates and fabrication of transistors thereof)
IT Glass substrates
(surface leveling with polymer reflowing; thin-film transistors having polycrystal silicon on glass substrates and fabrication of transistors thereof)
IT Semiconductor materials
(thin film, polycryst.; thin-film transistors having polycrystal silicon on glass substrates and fabrication of

transistors thereof)
IT   Thin film transistors
(thin-film transistors having polycrystal silicon on glass substrates and fabrication of transistors thereof)
IT   7440-42-8, Boron, uses   7723-14-0, Phosphorus, uses
(dopant in silica, for control of glass transition temp.; thin-film transistors having polycrystal silicon on glass substrates and fabrication of transistors thereof)
IT   109371-84-8, Silicon nitride (Si0-1N0-1)
(multilayer diffusion barrier; thin-film transistors having polycrystal silicon on glass substrates and fabrication of transistors thereof)
IT   7440-21-3, Silicon, properties
(polycryst., circuit formation on glass substrate; thin-film transistors having polycrystal silicon on glass substrates and fabrication of transistors thereof)
IT   7631-86-9P, Silica, properties
(surface leveled materials; thin-film transistors having polycrystal silicon on glass substrates and fabrication of transistors thereof)
OSC.G   1   THERE ARE 1 CAPLUS RECORDS THAT CITE THIS RECORD (1 CITINGS)

L132 ANSWER 6 OF 17 HCA COPYRIGHT 2011 ACS on STN
AN   133:25406 HCA Full-text
TI   Etching of contact holes in buffer layer in semiconductor device fabrication
IN   Li, Li; Wu, Zhiqiang; Parekh, Kunal R.
PA   Micron Technology, Inc., USA
SO   U.S., 13 pp.
CODEN: USXXAM
DT   Patent
LA   English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6077790	A	20000620	US 1997-818325	19970314
	US 6191047	B1	20010220	US 2000-597189	20000620
	US 20010009810	A1	20010726	US 2001-785728	20010216
	US 6495471	B2	20021217		
PRAI	US 1997-818325	A1	19970314		
	US 2000-597189	A1	20000620		

ASSIGNMENT HISTORY FOR US PATENT AVAILABLE IN LSUS DISPLAY FORMAT
AB   The present invention is directed toward building a microelectronic device in which a semiconductor substrate has thereon an etch buffer layer used in a processing method in which the buffer layer will act as an etch uniformity aid. In a method of making the microelectronic device, a semiconductor substrate is covered with an etch buffer layer and with an insulative layer. A first etch is performed by patterning and etching through a mask. The first etch penetrates the insulative layer, forms a cavity therein, and is selective to the buffer layer so as to expose the buffer layer. A second

etch is performed that is selective to the insulative layer and the semiconductor substrate, and is not selective to the buffer layer. The buffer layer can be an insulative material of a type other than the material of the insulative layer or the buffer layer can also be of a conductive material. Where the buffer layer is of a conductive layer, the effect of the second etch is that the insulative layer is substantially undercut due to the etching of the buffer layer and due to selectivity to all other etch-exposed structures upon the semiconductor substrate. The undercut leaves a laterally-oriented second cavity within which lateral surfaces of the buffer layer are exposed. Following the second etch, a method of covering the laterally exposed surfaces of the buffer layer, exposed by the undercut, is chosen in order to isolate the remaining laterally exposed surfaces of the buffer layer. These methods include reflowing the insulative layer to cover the laterally exposed surfaces of the buffer layer, and forming a liner layer in the cavity to cover the laterally exposed surfaces of the buffer layer.

CC 76-3 (Electric Phenomena)

IT Phosphosilicate glasses
(etching of contact holes in buffer layer in fabrication of semiconductor devices contg.)

IT Borophosphosilicate glasses
(insulating layers; etching of contact holes in fabrication of semiconductor device contg.)

OSC.G 4 THERE ARE 4 CAPLUS RECORDS THAT CITE THIS RECORD (4 CITINGS)

RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L132 ANSWER 7 OF 17 HCA COPYRIGHT 2011 ACS on STN

AN 131:345278 HCA Full-text

TI Semiconductor device having tungsten plug and its manufacture

IN Kinashi, Koji

PA Nippon Steel Corp., Japan

SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
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PI	JP 11317407	A	19991116	JP 1998-122423	19980501
PRAI	JP 1998-122423		19980501		

AB The device is equipped with a BPSG layer having a contact hole and a W film in the hole on a semiconductor substrate, in which diam. of the hole gradually increases from its upper part to its bottom and an impurity concn. in the layer gradually increases from the upper part to the bottom. The manuf. method involves (1) forming the layer on a device-formed semiconductor substrate , (2) etching to form the hole to the substrate in the layer, (3) forming the film on the substrate, and (4) planarizing the film. The hole has an appropriate structure for burying the W film, so that the device with high reliability can be manufd. by the method. IPCI H01L0021-3205 [ICM,6]; H01L0021-28 [ICS,6]; H01L0021-768 [ICS,6]

IPCR H01L0021-02 [I,C*]; H01L0021-28 [I,A]; H01L0021-3205 [I,A];

H01L0021-70 [I,C*]; H01L0021-768 [I,A]
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 75
ST semiconductor device tungsten plug formation; multilayer metal wiring semiconductor device fabrication
IT 7631-86-9P, Silica, uses
(boron- and phosphorus-doped; manuf. of semiconductor device having W plug-buried contact hole)

L132 ANSWER 8 OF 17 HCA COPYRIGHT 2011 ACS on STN
AN 130:290268 HCA Full-text
TI Techniques for forming electrically blowable fuses in an integrated circuit
IN Weigand, Peter; Tobben, Dirk
PA Siemens A.-G., Germany
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5899736	A	19990504	US 1997-933955	19970919
	EP 903784	A2	19990324	EP 1998-112434	19980704
	EP 903784	A3	20050323		
	EP 903784	B1	20070418		
	CN 1212457	A	19990331	CN 1998-118680	19980825
	CN 1129187	C	20031126		
	JP 11150190	A	19990602	JP 1998-263009	19980917
PRAI	US 1997-933955	A	19970919		

ASSIGNMENT HISTORY FOR US PATENT AVAILABLE IN LSUS DISPLAY FORMAT
AB A method for fabricating an elec. blowable fuse on a semiconductor substrate includes forming a fuse portion on the semiconductor substrate. The fuse portion is configured to turn substantially nonconductive when a current exceeding a predefined current level passes through the fuse portion. The method also includes depositing a substantially conformal 1st layer of dielec. material above the fuse portion and depositing a 2nd layer of a different dielec. material above the 1st layer, forming a protrusion of dielec. material above the fuse portion. The protrusion is chem.-mech. polished to form an opening through the 2nd layer above the protrusion. There is also included etching, in a substantially isotropic manner, a portion of the 1st layer through the opening to form a microcavity about the fuse portion. The etching is substantially selective to the 2nd layer and the fuse portion. Addnl., a substantially conformal 3rd layer of dielec. material is deposited above the 2nd layer, closing the opening in the 2nd layer.
CC 76-3 (Electric Phenomena)
IT Borophosphosilicate glasses
Metals, processes
Phosphosilicate glasses
(forming elec. blowable fuses in integrated circuits contg.)
OSC.G 3 THERE ARE 3 CAPLUS RECORDS THAT CITE THIS RECORD (3 CITINGS)

RE.CNT 2   THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
               ALL CITATIONS AVAILABLE IN THE RE FORMAT

L132 ANSWER 9 OF 17 HCA COPYRIGHT 2011 ACS on STN
AN   127:256280 HCA Full-text
OREF 127:49921a,49924a
TI   Gettered semiconductor substrates and fabrication
     thereof for prevention of releasing gettered impurities
IN   Horikawa, Tsuguhiro
PA   NEC Corp., Japan
SO   Jpn. Kokai Tokkyo Koho, 7 pp.
     CODEN: JKXXAF
DT   Patent
LA   Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09223698	A	19970826	JP 1996-29652	19960216
	JP 2743904	B2	19980428		
	US 5973386	A	19991026	US 1997-800235	19970212
PRAI	JP 1996-29652	A	19960216		

ASSIGNMENT HISTORY FOR US PATENT AVAILABLE IN LSUS DISPLAY FORMAT
AB   The title fabrication involves laminating on a rear surface of a p-Si substrate alternately with B-doped Si layers and SiO_2 layers wherein B concn. becomes higher along the lamination, annealing the substrate laminate for increased gettering concn. in higher Si layers, and subsequently removing the higher Si layers which contain higher concn. of gettered impurities. The removal of the higher Si layers prevents releasing of gettered impurities in heating process thereafter. IPCI H01L0021-322 [ICM,6]; H01L0021-322 [ICS,6]; H01L0021-02 [ICS,6,C*]
IPCR H01L0021-02 [I,C*]; H01L0021-322 [I,A]
CC   76-3 (Electric Phenomena)
ST   gettered semiconductor substrate impurity
     releasing prevention
IT   Semiconductor materials
        (gettered semiconductor substrates and
        fabrication thereof for prevention of releasing gettered
        impurities)
IT   Impurities
        (gettered, releasing prevention; gettered semiconductor
        substrates and fabrication thereof for prevention of
        releasing gettered impurities)
IT   Getters
        (releasing prevention; gettered semiconductor
        substrates and fabrication thereof for prevention of
        releasing gettered impurities)
IT   7440-21-3, Silicon, properties
        (boron-doped, gettering layers; gettered semiconductor
        substrates and fabrication thereof for prevention of
        releasing gettered impurities)
IT   7440-42-8, Boron, uses
        (dopant; gettered semiconductor substrates and

fabrication thereof for prevention of releasing gettered impurities)
IT 7631-86-9, Silica, processes
(elec. insulator; gettered semiconductor substrates and fabrication thereof for prevention of releasing gettered impurities)

L132 ANSWER 10 OF 17 HCA COPYRIGHT 2011 ACS on STN
AN 124:133023 HCA Full-text
OREF 124:24439a,24442a
TI Multilayered transparent conductive film and touch-panel for writing with pen
IN Aizawa, Mamoru; Saito, Kazunori; Kawamura, Kyoshi; Saito, Noryoshi
PA Nippon Soda Co, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07257945	A	19951009	JP 1994-73906	19940318
PRAI	JP 1994-73906		19940318		

AB The film consists of a transparent substrate successively coated with SiO_2, a transparent conductive film, and a transparent thin film with n ≤1.6 and has a transmittance (at 550 nm) ≥90% and surface resistivity 200-3000 Ω/.box.. The transparent thin film may comprise SiO_2 contg. P and/or B. The conductive film may comprise In oxide or Sn oxide contg. dopants. The substrate may be soda-lime glass. A touch panel using the conductive film is also claimed.
CC 76-2 (Electric Phenomena)
Section cross-reference(s): 38, 73
IT Polysilanes
(manuf. of silica composite multilayer transparent conductive film)
IT Electric conductors
(transparent, manuf. of metal oxide-silica multilayer transparent conductive film)
IT 7440-42-8, Boron, uses 7723-14-0, Phosphorus, uses
(dopant; manuf. of silica composite multilayer transparent conductive film)
IT 98387-81-6P
(manuf. of silica composite multilayer transparent conductive film)
IT 1332-29-2, Tin oxide 7631-86-9, Silica, processes 50926-11-9, ITO
(manuf. of silica composite multilayer transparent conductive film)
IT 7429-90-5, Aluminum, uses 7439-92-1, Lead, uses 7439-95-4, Magnesium, uses 7440-03-1, Niobium, uses 7440-21-3, Silicon, uses 7440-24-6, Strontium, uses 7440-25-7, Tantalum, uses 7440-31-5,

     Tin, uses   7440-32-6, Titanium, uses   7440-36-0, Antimony, uses
     7440-38-2, Arsenic, uses   7440-39-3, Barium, uses   7440-43-9,
     Cadmium, uses   7440-56-4, Germanium, uses   7440-62-2, Vanadium, uses
     7440-66-6, Zinc, uses   7440-67-7, Zirconium, uses   7440-69-9,
     Bismuth, uses   7440-70-2, Calcium, uses   7440-74-6, Indium, uses
     7782-41-4, Fluorine, uses
        (metal oxide dopant; manuf. of silica composite multilayer
        transparent conductive film)

L132 ANSWER 11 OF 17 HCA COPYRIGHT 2011 ACS on STN
AN   123:99905 HCA Full-text
OREF 123:17523a,17526a
TI   Manufacture of semiconductor devices
IN   Mizoguchi, Shuji; Fujiwara, Takumasa; Yoshimura, Naoaki
PA   Matsushita Electronics Corp, Japan
SO   Jpn. Kokai Tokkyo Koho, 4 pp.
     CODEN: JKXXAF
DT   Patent
LA   Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 06349769	A	19941222	JP 1993-137361	19930608
PRAI	JP 1993-137361		19930608		

AB   The manufg. process comprises the steps of: forming a SiO2 layer doped with B and/or P on a Si wafer; immersing the laminate in an eq. soln. contg. H2O2 and NH3 for forming a hydrophilic surface on the SiO2 layer; and forming contact holes in the SiO2 layer using a wet etching and then an anisotropic dry etching.
IPCI H01L0021-28 [ICM,5]; H01L0021-306 [ICS,5]; H01L0021-02 [ICS,5,C*];
     H01L0021-90 [ICS,5]
IPCR H01L0021-02 [I,C*]; H01L0021-28 [I,A]; H01L0021-306 [I,A]; H01L0021-70
     [I,C*]; H01L0021-768 [I,A]
CC   76-3 (Electric Phenomena)

L132 ANSWER 12 OF 17 HCA COPYRIGHT 2011 ACS on STN
AN   120:287535 HCA Full-text
OREF 120:50421a,50424a
TI   Manufacture of semiconductor devices
IN   Oota, Hiroyuki
PA   Fujitsu Ltd, Japan
SO   Jpn. Kokai Tokkyo Koho, 5 pp.
     CODEN: JKXXAF
DT   Patent
LA   Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 05326493	A	19931210	JP 1992-124562	19920518
PRAI	JP 1992-124562		19920518		

AB   In formation of nondoped glass layer on unlevelled substrate surface; Si alkoxide is bubbled with H gas for substitution of Me or Et groups with H to form OH and then the substrate is contacted with the alkoxide and O3 to form nondoped

glass layer. Formation of P doped glass or B- and P-doped glass layers are formed by using P alkoxide and optionally B alkoxide with Si alkoxide in the above process. Flat insulation layers are formed. IPCI H01L0021-316 [ICM,5]; C04B0041-85 [ICS,5]; H01L0021-312 [ICS,5];
H01L0021-3205 [ICS,5]; H01L0021-02 [ICS,5,C*]
IPCR C04B0041-85 [I,C*]; C04B0041-85 [I,A]; H01L0021-02 [I,C*];
H01L0021-312 [I,A]; H01L0021-316 [I,A]; H01L0021-3205 [I,A]
CC 76-3 (Electric Phenomena)
IT Glass, oxide
(borophosphosilicate, prepn. of, from silicon alkoxide and ozone, in semiconductor fabrication)
IT Glass, oxide
(phosphosilicate, prepn. of, from silicon alkoxide and ozone, in semiconductor fabrication)
IT 1333-74-0, Hydrogen, uses
(bubbling with, of alkoxides in glass insulator formation in semiconductor fabrication)

L132 ANSWER 13 OF 17 HCA COPYRIGHT 2011 ACS on STN
AN 117:162330 HCA Full-text
OREF 117:27817a,27820a
TI Method of etching and/or leveling the surface of a laminated semiconductor substrate
IN Sato, Fumihide
PA NEC Corp., Japan
SO Eur. Pat. Appl., 8 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 494745	A2	19920715	EP 1992-300080	19920106
	EP 494745	A3	19940316		
	EP 494745	B1	19991103		
	JP 06045327	A	19940218	JP 1991-795	19910109
	US 5272115	A	19931221	US 1991-816035	19911230
PRAI	JP 1991-795	A	19910109		

ASSIGNMENT HISTORY FOR US PATENT AVAILABLE IN LSUS DISPLAY FORMAT
AB Disclosed is an improved method of leveling the laminated surface of a semiconductor substrate, which method permits the exact controlling of the eating-out of the lamination on the semiconductor substrate by detecting the sudden change of the amt. of the gas resulting from the chem. reaction of the materials of the different layers with particular selected elements of surrounding plasma gas, thus assuring the reproducibility of leveled semiconductor substrate surface.
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 79
ST etching leveling surface semiconductor
IT 7440-42-8, Boron, uses 7723-14-0, Phosphorus, uses
(dopant, in silica, plasma etching of, in

semiconductor device manuf.)
IT 7631-86-9, Silicon oxide, uses
(phosphorus- and boron-doped, plasma
etching of, in semiconductor device manuf.)
OSC.G 20 THERE ARE 20 CAPLUS RECORDS THAT CITE THIS RECORD (20 CITINGS)

L132 ANSWER 14 OF 17 HCA COPYRIGHT 2011 ACS on STN
AN 116:226077 HCA Full-text
OREF 116:38061a,38064a
TI Manufacture of multilayer circuits in semiconductor devices
IN Ichiki, Hidehiko
PA Miyazaki Oki Electric Co., Ltd., Japan; Oki Electric Industry Co., Ltd.
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 03288438	A	19911218	JP 1990-89188	19900405
PRAI	JP 1990-89188		19900405		

AB The title manufg. method involves the following steps: (1) forming a silica film on a semiconductor substrate by deposition, (2) spin coating a silica film, forming a B-P-doped silica film by deposition, and reflowing, (3) forming a contact hole in the doped film and forming an interconnection groove in the doped film by etching over a resist mask, (4) removing the resist, forming a refractory metal silicide and an Al alloy, and melting the alloy at a high temp., (5) etching back the alloy over a dummy film, and (6) forming a silica film by deposition. The step coverage of the contact hole is improved.
IPCI H01L0021-3205 [ICM,5]; H01L0021-02 [ICM,5,C*]; H01L0021-90 [ICS,5]
IPCR H01L0021-02 [I,C*]; H01L0021-3205 [I,A]; H01L0021-70 [I,C*]; H01L0021-768 [I,A]; H01L0023-52 [I,C*]; H01L0023-52 [I,A]
CC 76-2 (Electric Phenomena)
Section cross-reference(s): 57
ST multilayer circuit interconnection semiconductor device
IT Glass, oxide
(borophosphosilicate, film, in manuf. of multilayer
circuit interconnection in semiconductor devices)
IT Electric circuits
(multilayer, manuf. of, interconnection in)
IT 11145-30-5
(elec. contacts, manuf. of multilayer interconnection
having, of semiconductor devices)

L132 ANSWER 15 OF 17 HCA COPYRIGHT 2011 ACS on STN
AN 115:266327 HCA Full-text
OREF 115:45073a,45076a
TI Low-loss waveguides on silicon substrates for
photonic circuits

AU   Davis, R. L.; Lee, S. H.
CS   Northrop Res. Technol. Cent., Palos Verdes Peninsula, CA, 90274, USA
SO   Proceedings of SPIE-The International Society for Optical Engineering
     (1991), 1474(Opt. Technol. Signal Process. Syst.), 20-6
     CODEN: PSISDG; ISSN: 0277-786X
DT   Journal
LA   English
AB   Techniques were developed for fabricating extremely low-loss channel waveguide structures on Si substrates. Waveguides were made and evaluated consisting of combinations of Corning 7059 glass, P-doped silica glass (PSG), and B-doped silica glass (BSG). The waveguides were fabricated on the surfaces of oxidized Si wafers. The 7059 waveguides were patterned in RF-sputter-deposited films, and the PSG waveguides were made using atm.-pressure, chem. vapor deposition (APCVD), low-pressure, chem. vapor deposition (LPCVD), and plasma-enhanced, chem. vapor deposition (PECVD). BSG was used strictly as a cladding layer for many of the waveguides. A comparison is given of the waveguides prepd. by these methods, and the processing techniques used to make channel waveguides with propagation losses less than 0.01 dB/cm are discussed. The processes used allowed making waveguides with cross-sections ranging from rectangular to nearly circular, and to build multiguide structures with the waveguides stacked vertically or arranged side by side. Applications for these waveguides include low-loss splitters and combiners, high-finesse resonators, switches, and wavelength division multiplexers/demultiplexers.
CC   73-11 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)
ST   glass waveguide silicon substrate photonic circuit
IT   Optical instruments
        (circuits, photonic, low-loss-waveguides on silicon substrates for)
IT   Waveguides
        (optical, fabrication of low-loss glass, on silicon substrates for photonic curcuits)
OSC.G   3   THERE ARE 3 CAPLUS RECORDS THAT CITE THIS RECORD (3 CITINGS)

L132 ANSWER 16 OF 17 HCA COPYRIGHT 2011 ACS on STN
AN   114:238754 HCA Full-text
OREF 114:40093a,40096a
TI   Manufacture of semiconductor device
IN   Yoshikawa, Kuniyoshi
PA   Toshiba Corp., Japan
SO   Jpn. Kokai Tokkyo Koho, 6 pp.
     CODEN: JKXXAF
DT   Patent
LA   Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 02126684	A	19900515	JP 1988-280632	19881107
PRAI	JP 1988-280632		19881107		

AB   A method for manufg. a semiconductor device involves the following steps: (1) forming a field insulating film between islands on a 1st cond. type

semiconductor substrate and gate insulating films on the islands; (2) forming a 1st polycryst. Si film (for a 1st gate electrode), a 2nd gate insulating film, and a 3rd polycryst. Si film (for a 2nd gate electrode) on the entire surface, followed by patterning the 3 films to form the 1st gate electrode, 2nd gate insulating film, and 2nd electrode in a self-aligned fashion; (3) forming a 3rd insulating film on the entire surface; (4) removing a part of the 3rd insulating film to expose the 2nd gate electrode; and (5) forming a 3rd electrode layer which is connected to the 2nd polycryst. Si film, followed by selective patterning of the 3rd electrode layer. The 3rd electrode layer can be a polycryst. Si film (or laminated layer with a silicide film). The 2nd gate insulating film can be Si oxide film (or its composite with Si nitride film). The 3rd insulating film can be a Si oxide film optionally doped with P, As, or B. The device shows an improved withstand voltage.

CC 76-3 (Electric Phenomena)

OSC.G 1 THERE ARE 1 CAPLUS RECORDS THAT CITE THIS RECORD (1 CITINGS)

L132 ANSWER 17 OF 17 HCA COPYRIGHT 2011 ACS on STN

AN 109:65484 HCA Full-text

OREF 109:10803a,10806a

TI Cap annealing in semiconductor device fabrication

IN Nishibori, Kazuya

PA Toshiba Corp., Japan

SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 63086426	A	19880416	JP 1986-229737	19860930
PRAI	JP 1986-229737		19860930		

AB A bilayered film comprising a phosphosilicate glass (PSG) film or a borophosphosilicate glass (BPSG) film with a Si_3N_4 film is used as a protective film for annealing after ion implantation in compd. semiconductor device fabrication. The protective film prevents the compd. semiconductor element diffusion and is useful for GaAs-based metal-semiconductor FET fabrication. A semi-insulating GaAs substrate implanted with Si was coated with a BPSG film by chem. vapor deposition (CVD) and a Si_3N_4 film by plasma CVD, and annealed in N_2 at 800° for 60 min to activate the ion implanted layer. No cracks or bubbles were obsd. in the annealing.

CC 76-3 (Electric Phenomena)

ST cap annealing protective film; phosphosilicate silicon nitride cap annealing; borophosphosilicate silicon nitride cap annealing; metal semiconductor FET cap annealing

IT Glass, oxide
(borophosphosilicate, protective bilayer film with layers of silicon nitride and, for cap annealing in FET fabrication)

IT Glass, oxide
(phosphosilicate, protective bilayer film with layers of silicon nitride and, for cap annealing in FET fabrication)

OSC.G 1 THERE ARE 1 CAPLUS RECORDS THAT CITE THIS RECORD (1 CITINGS)

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L133 ANSWER 1 OF 19  WPIX COPYRIGHT 2011       THOMSON REUTERS on STN
AN   2006-812734 [200682]   WPIX  Full-text
CR   2006-180657
DNC  C2006-256508 [200682]
DNN  N2006-623520 [200682]
TI   Backside contact solar cell manufacture, for electrical energy
     generation, involves diffusing dopants from boron-
     doped silicon diode, phosphorus-doped
     silicon dioxide and phosphorus into wafer
     via in-situ
DC   L03; U12
IN   CUDZINOVIC M J; MCINTOSH K R; MEHTA B G; SMITH D D
PA   (SUNP-N) SUNPOWER CORP
CYC  1
PI   US 7135350      B1 20061114 (200682)* EN  7[7]
ADT  US 7135350 B1 Provisional US 2003-508772P 20031003; US
     7135350 B1 Cont of US 2004-946564 20040921; US 7135350 B1 US
     2006-328419 20060109
FDT  US 7135350 B1 Cont of US 6998288 B
PRAI US 2006-328419       20060109
       US 2003-508772P      20031003
     US 2004-946564       20040921
AB    US 7135350 B1    UPAB: 20061222
       NOVELTY - A phosphorus-doped silicon dioxide layer (501) is laminated to a
      boron -doped silicon dioxide layer (104) at the backside of a silicon wafer
      (102). A solar cell has p-type and n-type regions (702,703) formed by
      diffusing dopants from the boron-doped and phosphorus-doped silicon dioxide
      , while phosphorus is diffused as n-type dopants (701) into the wafer
      through a front side. Diffusion of dopants is performed in-situ.
             USE - For manufacturing backside contact solar cell used to produce
      electrical energy from solar radiation.
             ADVANTAGE - Improves solar radiation collection efficiency by wet
      etching the front side of wafer to form a textured front side. Enhances
      protection of material at the backside of the wafer from texturing solution
      by forming an undoped oxide. Simplifies manufacturing process by using in-
      situ steps to drive dopants into the wafer.
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DESCRIPTION OF DRAWINGS - The figure shows the cross-section of the backside contact solar cell during manufacture.
Silicon wafer (102)
Boron-doped silicon dioxide layer (104)
Phosphorus-doped silicon dioxide layer (501)
N-type dopants (701)
P-type and n-type regions (702,703)

FS CPI; EPI
MC CPI: L03-E05B; L04-C02D
EPI: U12-A02A3
TT TT: BACKSIDE CONTACT SOLAR CELL MANUFACTURE ELECTRIC ENERGY GENERATE DIFFUSION DOPE BORON SILICON DIODE PHOSPHORUS WAFER SITU

L133 ANSWER 2 OF 19 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
AN 2006-152061 [200616] WPIX Full-text
CR 2003-707531; 2004-660470; 2005-119745; 2006-535400
DNC C2006-051413 [200616]
DNN N2006-131227 [200616]
TI Filling gaps on semiconductor substrate for electronic device fabrication comprises introducing process gas comprising hydrogen and phosphorus dopant precursor into process chamber of high density plasma chemical vapor deposition reactor
DC L03; U11; V05
IN HALL L; PAPASOULIOTIS G D; PRICHARD K; RAHMAN M S; SINGH V; SUN P S
PA (NOVE-N) NOVELLUS SYSTEMS INC
CYC 1
PI US 7001854 B1 20060221 (200616)* EN 15[6]
ADT US 7001854 B1 Provisional US 2001-310004P 20010803; US 7001854 B1 CIP of US 2001-996619 20011128; US 7001854 B1 US 2002-271333 20021011
FDT US 7001854 B1 CIP of US 6596654 B
PRAI US 2002-271333 20021011
US 2001-310004P 20010803
US 2001-996619 20011128
AB US 7001854 B1 UPAB: 20060308

NOVELTY - Filling gaps on a semiconductor substrate comprises providing a substrate in a process chamber of a high density plasma chemical vapor deposition reactor; and introducing a process gas comprising hydrogen and a phosphorus dopant precursor into the process chamber, in which the flow rate ratio of hydrogen gas to all other process gas constituents is in excess of 1:1.

DETAILED DESCRIPTION - Filling gaps on a semiconductor substrate comprises providing a substrate in a process chamber of a high density plasma chemical vapor deposition reactor; introducing a process gas comprising hydrogen (H2) and a phosphorus dopant precursor into the process chamber, in which the flow rate ratio of H2 to all other process gas constituents is in excess of 1:1; and applying a bias to the substrate, to grow a phosphorus-doped dielectric film via high density plasma chemical vapor deposition (HDP CVD) on the semiconductor substrate, in which the dielectric film fills gaps with a width of less than ca. 1.5 microns.

USE - Used for filling gaps on a semiconductor substrate for electronic device fabrication.

ADVANTAGE - Providing hydrogen as a phosphosilicate glass (PSG) process gas in a high density plasma CVD process results in void-free high-quality gap filling with phosphorus-containing dielectric materials. These benefits occur even in very narrow, high aspect ratio features.

DESCRIPTION OF DRAWINGS - The figure shows (a) a rough schematic cross-sectional diagram of a trench or via having problematic side-wall deposition of so dielectric during HDP CVD and (b) a rough schematic cross-sectional diagram of a trench or via having much less side-wall deposition of dielectric because the dielectric was grown with a hydrogen-containing PSG process gas.

Dielectric material (205)

Sputtered species (207)

Sidewalls (209)

Side dielectric (211', 211)

TECH CERAMICS AND GLASS - Preferred Materials: The dielectric film comprises a phosphorus-doped silicon oxide, phosphorus-doped silicon dioxide (SiO_2), phosphorus-doped silicon oxyfluoride, phosphorus-doped silicon oxynitride, phosphorus-doped and fluorine and nitrogen-containing silicon oxide, or phosphorus and boron-doped silicon oxide (BPSG).

CHEMICAL ENGINEERING - Preferred Process: The silicon-containing compound is decomposed to allow plasma phase reacting of a silicon-containing reactant on the surface of the substrate. Applying a bias to the substrate comprises supporting the substrate on a substrate holder having an electrode supplying a radio frequency bias to the substrate. The radio frequency bias is generated by supplying the electrode with greater than or equal to 0.2 W/cm2 of power. A heat transfer gas is supplied between a surface of the substrate and a surface of the substrate holder on which the substrate is supported during the film growing. An oxygen-containing gas, a phosphorus-containing gas and/or a hydrogen-containing gas are plasma phase reacted in the gaps and polymer residues in the gap are removed prior to the film growing.

Preferred Conditions: The process gas comprises hydrogen having a flow rate of 10-5000 (preferably 200-1000) standard cubic centimeters per minute (sccm) and phosphine having a flow rate of 0.2-150 (preferably 2-8) sccm. The process chamber is maintained at not greater than 100 mTorr. The radio frequency bias applied to the substrate is at 100 kHz to 27 MHz. The substrate is placed on a substrate holder maintained at 30-1000degreesC. The substrate temperature is held at 450-550degreesC during the dielectric film growing. The flow rate ratio of H_2 to all other process gases is in excess of 2:1 (preferably in excess of 10:1).

ELECTRONICS - Preferred Components: The phosphorus-doped dielectric film fills a shallow trench isolation gap, wherein it has less than 2 wt.% phosphorus content. Alternatively, the phosphorus-doped dielectric film fills an inter-layer

dielectric gap, wherein it has greater than 2 (preferably 6-9) wt.% phosphorus content. The dielectric film fills gaps with a width of less than about 0.13 microns and an aspect ratio in excess of 3:1 (preferably 4:1 - 10:1).

INORGANIC CHEMISTRY - Preferred Compounds: The process gas may further comprise a silicon-bearing compound, preferably silane (SiH_4), tetrafluorosilane (SiF_4), or disilane (Si_2H_6). The process gas further comprises nitrogen gas (N_2), nitrous oxide (N_2O), nitric oxide (NO), ammonia (NH_3), nitrogen trifluoride (NF_3), and/or oxygen gas (O_2). The phosphorus dopant precursor is phosphine or phosphorus pentafluoride. The heat transfer gas comprises helium and/or argon. The gas includes silicon and fluorine-containing reactants, nitrogen-containing reactants, silicon and reactant(s) containing fluorine and nitrogen, or boron-containing reactants.

MECHANICAL ENGINEERING - Preferred Components: The HDP CVD reactor comprises an electrode that generates a plasma from the process gas. The substrate is clamped on an electrostatic or mechanical chuck during the film growing. The process gas is introduced through a gas supply including orifices. At least some of the orifices orienting the process gas along an axis of injection intersecting an exposed surfaced of the substrate at an acute angle. Introducing the process gas comprises supplying a gas or gas mixture from a primary gas ring, wherein at least some of said gas or gas mixture is directed toward said substrate. Injectors are connected to the primary gas ring. The injectors injecting at least some of said gas or gas mixture into said chamber and directed toward substrate.

ORGANIC CHEMISTRY - Preferred Compounds: The process gas may further comprise a silicon-bearing compound, preferably tetraethyl orthosilicate (TEOS), tetramethyl-cyclotetrasiloxane (TMCTS), octamethyl-cyclotetrasiloxane (OMCTS), methyl-silane, dimethyl-silane, trimethylsilane (3MS), tetramethylsilane (4MS), tetramethyl-disiloxane (TMDSO), tetramethyl-diethoxyldisiloxane (TMDDSO), or dimethyl-dimethoxylsilane (DMDMS).

FS CPI; EPI

MC CPI: L04-C01B
EPI: U11-C05B2; U11-C05B7; V05-F05C; V05-F05E5; V05-F08D1

TT TT: FILL GAP SEMICONDUCTOR SUBSTRATE ELECTRONIC DEVICE FABRICATE COMPRISE INTRODUCING PROCESS GAS HYDROGEN PHOSPHORUS DOPE PRECURSOR CHAMBER HIGH DENSITY PLASMA CHEMICAL VAPOUR DEPOSIT REACTOR

AN 2005-511197 [200552] WPIX Full-text

CR 2004-293636; 2005-530179

DNC C2005-155087 [200552]

DNN N2005-417051 [200552]

TI Semiconductor device fabrication method e.g. for dynamic random access memory, involves forming etch stopper covering gate pattern and semiconductor substrate to predetermined thickness using low temperature atomic layer deposition

DC L03; U11; U14

IN CHU K; LEE J; PARK J; YANG J

PA (CHUK-I) CHU K; (LEEJ-I) LEE J; (PARK-I) PARK J; (YANG-I) YANG J
CYC 1
PI US 20050142781 A1 20050630 (200552)* EN 8[7]
ADT US 20050142781 A1 Cont of US 2003-612028 20030702; US 20050142781 A1 US 2004-24579 20041229
FDT US 20050142781 A1 Cont of US 6858533 B
PRAI KR 2002-55005 20020911
AB US 20050142781 A1 UPAB: 20051223

NOVELTY - An etch stopper (120) which covers the gate pattern (110) and the semiconductor substrate (100), is formed to a predetermined thickness using low temperature atomic layer deposition. The self-aligned contact hole (150) is formed by dry etching the interlayer insulating film (130) using the gate pattern as a mask. The etch stopper which is exposed to the self-aligned contact hole is removed by wet etching.

USE - For fabricating semiconductor device e.g. dynamic random access memory (DRAM)

ADVANTAGE - Recess if the semiconductor substrate and damage are prevented.

DESCRIPTION OF DRAWINGS - The figure shows the sectional view of self-aligned contact (SAC) process of semiconductor device using a nitride film formed by low temperature atomic layee deposition (ALD) as an etch stopper.

semiconductor substrate (100)
gate pattern (110)
etch stopper (120)
interlayer insulating film (130)
self-aligned contact hole (150)

TECH INORGANIC CHEMISTRY - Preferred Component: The etch stopper film comprises a nitride film. Reaction gas used for forming the etch stopper, uses silicon hydrate (SiH_4), silicon chlorohy- drate ($SiCl_2H_2$) or silicon tetrachloride ($SiCl_4$) as silicon source, and nitrogen, ammonia or nitrous oxide as nitrogen source. The interlayer insulating film is a single layer oxide film or multilayer oxide film formed using silica (SiO_2), boron doped phosphosilicate glass (BPSG), high density polyethylene (HDP) oxide or flowable oxide (FOx). Hydrofluoric acid solution is used as etching solution during wet etching for removing the etch stopper.

ORGANIC CHEMISTRY - Preferred Component: The etch stopper film comprises a nitride film. Reaction gas used for forming the etch stopper, uses silicon hydrate (SiH_4), silicon chlorohy- drate ($SiCl_2H_2$) or silicon tetrachloride ($SiCl_4$) as silicon source, and nitrogen, ammonia or nitrous oxide as nitrogen source. The interlayer insulating film is a single layer oxide film or multilayer oxide film formed using silica (SiO_2), boron doped phosphosilicate glass (BPSG), high density polyethylene (HDP) oxide or flowable oxide (FOx). Hydrofluoric acid solution is used as etching solution during wet etching for removing the etch stopper.

FS CPI; EPI
MC CPI: L04-C06A; L04-C07B; L04-C13A; L04-E15
EPI: U11-C05B9A; U11-C18B5; U14-A03B7

TT   TT: SEMICONDUCTOR DEVICE FABRICATE METHOD DYNAMIC RANDOM ACCESS MEMORY
FORMING ETCH STOPPER COVER GATE PATTERN SUBSTRATE PREDETERMINED
THICK LOW TEMPERATURE ATOMIC LAYER DEPOSIT

L133 ANSWER 4 OF 19 WPIX COPYRIGHT 2011   THOMSON REUTERS on STN
AN   2005-433128 [200544]   WPIX Full-text
TI   Defining an opening in stack of insulator layers on semiconductor substrate for fabricating semiconductor devices, comprises forming opening in insulator layer to expose portion of top surface of tri-layer insulator composite
DC   L03; U11
IN   CHENG S; CHENG Y
PA   (TSMC-C) TAIWAN SEMICONDUCTOR MFG CO; (TSMC-C) TAIWAN SEMICONDUCTOR MFG CO LTD
CYC 2
PI   US 20050112859 A1 20050526 (200544)* EN 8[8]
     US 7074701   B2 20060711 (200646) EN
     TW 239565   B1 20050911 (200672) ZH
     TW 2005018223   A 20050601 (200962) ZH
ADT US 20050112859 A1 US 2003-718881 20031121; TW 239565 B1 TW 2004-128416 20040920; TW 2005018223 A TW 2004-128416 20040920
PRAI US 2003-718881   20031121
AB   US 20050112859 A1   UPAB: 20080523

NOVELTY - Defining an opening in stack of insulator layers on semiconductor substrate (1), comprises forming tri-layer insulator composite on conductive region and on portions of semiconductor substrate; forming insulator layer on tri-layer insulator composite; forming opening in insulator layer to expose portion of top surface of tri-layer insulator composite; and removing portion of tri-layer insulator composite exposed in opening.

DETAILED DESCRIPTION - Defining an opening in a stack of insulator layers on a semiconductor substrate, comprises:

(1) providing a conductive region (11) on the semiconductor substrate;

(2) forming a tri-layer insulator composite on the conductive region and on portions of the semiconductor substrate;

(3) forming an insulator layer on the tri- layer insulator composite;

(4) forming an opening in the insulator layer to expose a portion of a top surface of the tri-layer insulator composite; and

(5) removing portion of the tri-layer insulator composite exposed in the opening, exposing a portion of a top surface of the conductive region.

An INDEPENDENT CLAIM is also included for method of forming an opening in insulator layers, comprising:

(1) providing a semiconductor substrate;

(2) forming a conductive region on the semiconductor substrate;

(3) forming a tri-layer insulator over the conductive region and on the semiconductor substrate , with the tri-layer insulator comprised with a hydro-silicon oxynitride (HOxSN) middle layer;

(4) forming an insulator layer on the tri- layer insulator; and

(5) forming an opening in the insulator layer and in the tri-layer insulator to expose the conductive region.

USE - For defining an opening in a stack of insulator layers on a semiconductor substrate (claimed) used for fabricating semiconductor devices.

ADVANTAGE - The method employs a contact or via opening definition procedure featuring high etch rate selectivity between the overlying insulator layers and the underlying tri- layer insulator composite stop layer, to allow an extended insulator over etch cycle to be used to insure against thickness uniformity of the overlying insulator layer component of the stack of insulator layers.

DESCRIPTION OF DRAWINGS - The figure in cross-sectional style show a contact hole opening and via hole opening exposing underlying conductive regions of a semiconductor device.

Substrate (1)
Silicon oxide layer (3)
HOxSN layer (4)
Silicon nitride layer (5)
BPSG layer (6)
Conductive region (11)

TECH CERAMICS AND GLASS - Preferred Component: The insulator layer is composed of an underlying boro-phosphosilicate glass (BPSG) layer (6), obtained via PECVD or LPCVD procedures to a thickness of 1500-2500 Angstrom .

ELECTRONICS - Preferred Component: The conductive region is a source/drain region in a semiconductor substrate, or a metal structure such as a metal interconnect structure.

INORGANIC CHEMISTRY - Preferred Component: The tri- layer insulator layer is composed of an underlying silicon rich, silicon oxide layer (3), HOxSN layer (4), and an overlying silicon nitride layer (5).

Preferred Method: An underlying silicon rich, silicon oxide layer of the tri-layer insulator composite, is formed via low pressure chemical vapor deposition (LPCVD), via plasma enhanced chemical vapor deposition (PECVD), or via high density plasma chemical vapor deposition (HDPCVD) procedures, to a thickness of 100-200 Angstrom , using silane or disilane, and oxygen or nitrous oxide as reactants. The opening in the insulator layer is formed via a dry etch, anisotropic reactive ion etch (RIE) procedure, using trifluoromethane as an etchant for the insulator layer. A silicon nitride layer component of the tri-layer insulator composite is removed via an anisotropic RIE procedure using tetrafluoromethane or chlorine gas as an etchant.

Preferred Parameter: An underlying silicon rich, silicon oxide layer of the tri-layer insulator composite is comprised with a refractive index of 1.485-1.55.

ORGANIC CHEMISTRY - Preferred Component: The tri- layer insulator layer is composed of an underlying silicon rich, silicon oxide layer (3), HOxSN layer (4), and an overlying silicon nitride layer (5).

Preferred Method: An underlying silicon rich, silicon oxide layer of the tri-layer insulator composite, is formed via low pressure chemical vapor deposition (LPCVD), via plasma enhanced chemical vapor deposition (PECVD), or via

high density plasma chemical vapor deposition (HDPCVD) procedures, to a thickness of 100-200 Angstrom , using silane or disilane, and oxygen or nitrous oxide as reactants. The opening in the insulator layer is formed via a dry etch, anisotropic reactive ion etch (RIE) procedure, using trifluoromethane as an etchant for the insulator layer. A silicon nitride layer component of the tri-layer insulator composite is removed via an anisotropic RIE procedure using tetrafluoromethane or chlorine gas as an etchant.
Preferred Parameter: An underlying silicon rich, silicon oxide layer of the tri-layer insulator composite is comprised with a refractive index of 1.485-1.55.

FS CPI; EPI

MC CPI: L04-C01B; L04-C06B1; L04-C06C; L04-C07B; L04-C10; L04-C12A; L04-C12B; L04-C13A
EPI: U11-C05D1; U11-C05D3; U11-C05G2C; U11-C07C3

TT TT: DEFINE OPEN STACK INSULATE LAYER SEMICONDUCTOR SUBSTRATE FABRICATE DEVICE COMPRISE FORMING EXPOSE PORTION TOP SURFACE TRI COMPOSITE

L133 ANSWER 5 OF 19 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN

AN 2005-255305 [200527] WPIX Full-text

DNC C2005-081165 [200527]

DNN N2005-210068 [200527]

TI Fabrication of a multi-layer plate structure, notably for silicon on insulator wafers for micro-electronic applications involves heat treatment so that the intermediate layer deforms and micro-balls or micro-cavities are formed

DC L03; U11

IN BRUEL M

PA (BRUE-I) BRUEL M; (TRAC-N) TRACIT TECHNOLOGIES

CYC 107

PI

FR 2860249	A1	20050401	(200527)*	FR	24[6]
WO 2005034218	A2	20050414	(200527)	FR	
EP 1671361	A2	20060621	(200643)	FR	
JP 2007507872	T	20070329	(200725)	JA	19
EP 1671361	B1	20070404	(200726)	FR	
CN 1883031	A	20061220	(200730)	ZH	
DE 602004005731	E	20070516	(200734)	DE	
KR 2006117925	A	20061117	(200734)	KO	
DE 602004005731	T2	20071227	(200803)	DE	
US 20080038564	A1	20080214	(200813)	EN	
CN 100514560	C	20090715	(201001)	ZH	

ADT FR 2860249 A1 FR 2003-11450 20030930; CN 1883031 A CN 2004-80033848 20040923; DE 602004005731 E DE 2004-602004005731 20040923; DE 602004005731 T2 DE 2004-602004005731 20040923; EP 1671361 A2 EP 2004-787425 20040923; EP 1671361 B1 EP 2004-787425 20040923; DE 602004005731 E EP 2004-787425 20040923; DE 602004005731 T2 EP 2004-787425 20040923; WO 2005034218 A2 WO 2004-FR2398 20040923; EP 1671361 A2 WO 2004-FR2398 20040923; JP 2007507872 T WO 2004-FR2398 20040923; EP 1671361 B1 WO 2004-FR2398 20040923; KR 2006117925 A WO 2004-FR2398 20040923; DE 602004005731 E WO 2004-FR2398 20040923; DE

602004005731 T2 WO 2004-FR2398 20040923; US 20080038564 A1 WO 2004-FR2398 20040923; JP 2007507872 T JP 2006-530396 20040923; KR 2006117925 A KR 2006-708261 20060428; US 20080038564 A1 US 2007-574120 20070531; CN 100514560 C CN 2004-80033848 20040923

FDT DE 602004005731 E Based on EP 1671361 A; EP 1671361 A2 Based on WO 2005034218 A; JP 2007507872 T Based on WO 2005034218 A; EP 1671361 B1 Based on WO 2005034218 A; KR 2006117925 A Based on WO 2005034218 A; DE 602004005731 E Based on WO 2005034218 A; DE 602004005731 T2 Based on EP 1671361 A; DE 602004005731 T2 Based on WO 2005034218 A

PRAI FR 2003-11450 20030930

IPCI B29C0071-00 [I,A]; B29C0071-00 [I,C]; B32B0009-04 [I,A]; B32B0009-04 [I,C]; C30B0033-00 [I,C]; C30B0033-00 [I,C]; C30B0033-00 [I,C]; C30B0033-02 [I,A]; C30B0033-02 [I,A]; H01L0021-02 [I,A]; H01L0021-02 [I,C]; H01L0021-02 [I,C]; H01L0021-02 [I,C]; H01L0021-20 [I,A]; H01L0021-20 [I,A]; H01L0027-12 [I,A]; H01L0027-12 [I,C]

IPCR C30B0033-00 [I,A]; C30B0033-00 [I,C]; C30B0033-02 [I,A]; H01L0021-02 [I,C]; H01L0021-20 [I,A]; H01L0021-70 [I,C]; H01L0021-762 [I,A]

EPC C30B0033-00+29/06; C30B0033-02; H01L0021-762D8B

NCL NCLM 428/446.000
NCLS 257/E21.568; 264/345.000

FCL H01L0021-02 B; H01L0027-12 B; H01L0027-12 Z

FTRM 5F084; 5F117

AB FR 2860249 A1 UPAB: 20051221

NOVELTY - The fabrication of a plate structure with a substrate (2), a superstratum (3) and an intermediate layer (4), consists of:

(a) choosing an intermediate layer comprising a base material in which some extrinsic atoms or molecules, different from those of the base material, are distributed;

(b) heat treating the structure (1) such that, in the temperature range of this treatment, the intermediate layer is able to plastically deform and the presence of the extrinsic atoms or molecules in the base material generate, in an irreversible manner, the formation of micro-balls or micro-cavities in the intermediate layer.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) the fabrication of silicon platelets incorporating this structure;

(b) application of this method to the fabrication of Silicon On Insulator plates;

(c) a plate structure with a substrate, a superstratum and an intermediate layer.

USE - The invention is used for the fabrication of multi-layer plates and thin platelets, notably of Silicon On Insulator plates for micro-electronic and opto-electronic applications.

ADVANTAGE - The invention improves the techniques and the actual structures by improving their performance and thus diversifying their application.

DESCRIPTION OF DRAWINGS - The drawing is a cross-section of a structure in an ulterior stage of the fabrication according to the invention.

Multi-layer structure; (1)

Substrate; (2)

Superstratum; (2)
Intermediate layer; (4)
Film of thermal silicon oxide; (5)
Film of chemically cleaned or polished thermal silicon oxide. (6)

TECH CERAMICS AND GLASS - Preferred Materials: The base material of the intermediate layer is silica and the extrinsic atoms are of phosphorus or boron thus forming an intermediate layer of phospho-silicate-glass or boro-phospho-silicate-glass (claimed).

FS CPI; EPI

MC CPI: L04-C16
EPI: U11-C08A6

TT TT: FABRICATE MULTI LAYER PLATE STRUCTURE NOTABLY SILICON INSULATE WAFER MICRO ELECTRONIC APPLY HEAT TREAT SO INTERMEDIATE DEFORM BALL CAVITY FORMING

L133 ANSWER 6 OF 19 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN

AN 2005-100641 [200511] WPIX Full-text

DNC C2005-033644 [200511]

DNN N2005-087438 [200511]

TI Planarization of interlayer dielectric layer for DRAM comprises forming three interlayer dielectric layers having different etch selectivities and chemical mechanical polishing third and second layers

DC L03; U11; U13; U14

IN HONG C; HONG C K; LEE J; LEE J D; PARK J S; PARK Y; PARK Y R

PA (SMSU-C) SAMSUNG ELECTRONICS CO LTD

CYC 2

PI US 20050014330 A1 20050120 (200511)* EN 19[13]
KR 2005008364 A 20050121 (200535) KO

ADT US 20050014330 A1 US 2004-777864 20040212; KR 2005008364 A KR 2003-48432 20030715

PRAI KR 2003-48432 20030715

AB US 20050014330 A1 UPAB: 20060121

NOVELTY - Planarizing interlayer dielectric layer comprises forming first, second and third interlayer dielectric layers having different etching selectivities; and chemical mechanical polishing the third and second interlayer dielectric layers in the first region of the first interlayer dielectric layer using the third interlayer dielectric layer in the second region and the first interlayer dielectric layer in the first region as etching end points.

DETAILED DESCRIPTION - Planarizing an interlayer dielectric layer comprises forming a first interlayer dielectric layer over a first region in which a capacitor (170) is formed and a second region adjacent to the first region, wherein the first region is higher than the second region; forming a second interlayer dielectric layer over the first interlayer dielectric layer and having an etching selectivity different from that of the first interlayer dielectric layer; forming a third interlayer dielectric layer over the second interlayer dielectric layer and having an etching selectivity different from that of the second interlayer dielectric layer; and chemical mechanical polishing the third and second interlayer dielectric

layers in the first region using the third interlayer dielectric layer in the second region and the first interlayer dielectric layer in the first region as etching end points.

USE - For planarizing an interlayer dielectric layer formed over a one-cylinder storage (OCS) capacitor for DRAM.

ADVANTAGE - Double-interlayer dielectric layer structure is formed, instead of the triple- interlayer dielectric layer structure so that a simpler process is achieved. Because the photolithography process performed to expose the cell region is omitted, a simple process can be achieved, process throughput can be enhanced and manufacturing costs can be reduced. Because a selective chemical mechanical polishing process is carried out, in-wafer spread can be improved. Because the number of process steps is reduced, the possibility of defects occurring during manufacturing is also reduced, resulting in stable operation of a resulting semiconductor device.

DESCRIPTION OF DRAWINGS - The figure shows a cross-sectional view of an interlayer dielectric layer.

Semiconductor substrate (110)
Gates (120)
Insulating layers (125,135)
Contact pads (130)
Contact plug (145)
Lower electrode (155a)
Dielectric layer (160)
Upper electrode (165)
Capacitor (170)
Cell region (C)
Peripheral circuit region (P)

TECH CERAMICS AND GLASS - Preferred Materials: The first and third interlayer dielectric layers are made of flow fill, SiLK, silicon oxycarbide (SiOC), black diamond, CORAL, undoped polysilicon, silicon nitride (SiN), silicon oxynitride (SiON), boron nitride (BN), and/or anti-reflection coating. The second interlayer dielectric layer is made of plasma-enhanced oxide, undoped silicate glass, spin-on glass, flowable oxide, boro-phosphorus silicate glass, phosphorus silicate glass, and/or plasma-enhanced tetraethylorthosilicate. The slurry is a ceria slurry, silica slurry, mangania slurry, and/or alumina slurry.

ELECTRONICS - Preferred Components: The third interlayer dielectric layer has the same etching selectivity in the chemical mechanical polishing step as the first interlayer dielectric layer. The second interlayer dielectric layer has a lower etching selectivity in the chemical mechanical polishing step that the first and third interlayer dielectric layers. The third interlayer dielectric layer in the second region is higher than the first interlayer dielectric layer in the first region.

INORGANIC CHEMISTRY - Preferred Method: The third and second interlayer dielectric layers are chemical mechanical polished once using a slurry having an etching selectivity between the second and third interlayer dielectric layers that is greater than 5:1. The chemical mechanical polishing of the third and second

interlayer dielectric layers comprises removing the third interlayer dielectric layer in the first region using a first slurry that etches the third interlayer dielectric layer at a higher etch rate than that of the second interlayer dielectric layer; and removing the second interlayer dielectric layer in the first region using a second slurry that etches the second interlayer dielectric layer at a higher etch rate than that of the first and third interlayer dielectric layers.

ORGANIC CHEMISTRY - Preferred Method: The third and second interlayer dielectric layers are chemical mechanical polished once using a slurry having an etching selectivity between the second and third interlayer dielectric layers that is greater than 5:1. The chemical mechanical polishing of the third and second interlayer dielectric layers comprises removing the third interlayer dielectric layer in the first region using a first slurry that etches the third interlayer dielectric layer at a higher etch rate than that of the second interlayer dielectric layer; and removing the second interlayer dielectric layer in the first region using a second slurry that etches the second interlayer dielectric layer at a higher etch rate than that of the first and third interlayer dielectric layers.

FS CPI; EPI
MC CPI: L04-C14A; L04-C27; L04-E15
EPI: U11-C06A1A; U11-C18B5; U13-C04B1A; U14-A03B4
TT TT: PLANE INTERLAYER DIELECTRIC LAYER DRAM COMPRISE FORMING THREE ETCH SELECT CHEMICAL MECHANICAL POLISH THIRD SECOND

L133 ANSWER 7 OF 19 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
AN 2004-736557 [200472] WPIX Full-text
DNC C2004-258922 [200472]
DNN N2004-582872 [200472]
TI Fabrication of transistor for active matrix liquid crystal display, by patterning resist layer formed on seed layer to expose portions of the seed layer, and electrochemical depositing metal layer on the exposed portions
DC L03; U11; U12; U14
IN BACHRACH R Z; LAW K S; SHANG Q; WHITE J M
PA (BACH-I) BACHRACH R Z; (LAWK-I) LAW K S; (SHAN-I) SHANG Q; (WHIT-I) WHITE J M; (APMA-C) APPLIED MATERIALS INC
CYC 107

PI	US 20040203181	A1	20041014	(200472)*	EN	17[6]
	WO 2004093198	A1	20041028	(200472)	EN	
	US 6887776	B2	20050503	(200530)	EN	
	TW 297952	B1	20080611	(200924)	ZH	
	TW 2005007261	A	20050216	(200958)	ZH	

ADT US 20040203181 A1 US 2003-412620 20030411; WO 2004093198 A1 WO 2004-US11075 20040409; TW 297952 B1 TW 2004-110142 20040412; TW 2005007261 A TW 2004-110142 20040412
PRAI US 2003-412620 20030411
AB US 20040203181 A1 UPAB: 20060122

NOVELTY - A transistor is fabricated by forming a metal gate on a glass substrate. The step of forming the metal gate on the substrate involves depositing a conductive seed layer on a substrate surface, depositing a resist material on the conductive seed layer, patterning the resist layer to expose portions of the conductive seed layer, and depositing a metal layer on the exposed portions of the conductive seed layer using electrochemical deposition.

USE - For fabricating transistor for use in active matrix liquid crystal display (claimed) useful for computer monitors, television screens, camera displays, or avionics displays.

ADVANTAGE - The inventive method uses electrochemical deposition method to improve the deposition of the metal material on the substrate. It is capable of sequentially depositing layers without exposing the substrate to atmosphere between the seed layer and copper layer deposition steps to prevent oxidation.

DESCRIPTION OF DRAWINGS - The figure is a flow chart illustrating steps of depositing layers.

TECH CERAMICS AND GLASS - Preferred Material: The glass substrate comprises undoped silica glass (USG), phosphorus doped glass (PSG), boron-phosphorus doped glass (BPSG), soda-lime glass, borosilicate glass, sodium borosilicate glass, alkali-metal borosilicate, aluminosilicate glass, aluminoborosilicate glass, alkaline earth aluminoborosilicate glass, and/or alkaline earth-metal aluminoborosilicate glass.

ELECTRONICS - Preferred Method: The method includes removing the resist material, etching the exposed portions of the conductive seed layer, depositing dielectric layer(s) on the metal layer, and forming source region(s) and drain region(s) on the dielectric layers. The electrochemical deposition involves electroplating or electroless deposition. The method includes depositing a barrier layer on the substrate surface before the seed layer is deposited. The deposition of the seed layer involves thermal chemical vapor deposition, plasma chemical vapor deposition, atomic layer deposition, and/or evaporation. The source regions and drain regions are formed in doped semiconductor layers. Gate dielectric layers are formed on the doped semiconductor layers. The method includes depositing an interlayer dielectric material on the substrate and on the metal gates, patterning one or more gate dielectric layers and the interlayer dielectric material to form feature definitions exposing underlying source regions and drain regions, and depositing the metal layer in the feature definitions to form a contact.

INORGANIC CHEMISTRY - Preferred Material: The seed layer comprises a metal of copper, nickel, tungsten, molybdenum, cobalt, ruthenium, titanium, zirconium, hafnium, niobium, tantalum, vanadium, chromium, manganese, iron, palladium, platinum, and/or aluminum.

ORGANIC CHEMISTRY - Preferred Material: The seed layer comprises a metal of copper, nickel, tungsten, molybdenum, cobalt, ruthenium, titanium, zirconium, hafnium, niobium, tantalum, vanadium, chromium, manganese, iron, palladium, platinum, and/or aluminum.

FS CPI; EPI

MC CPI: L03-G05B; L04-C06B1; L04-C10; L04-C10D; L04-E01

EPI: U11-C18A1; U12-B03A; U14-K01A1J; U14-K01A2B
TT   TT: FABRICATE TRANSISTOR ACTIVE MATRIX LIQUID CRYSTAL DISPLAY PATTERN RESIST LAYER FORMING SEED EXPOSE PORTION ELECTROCHEMICAL DEPOSIT METAL

L133 ANSWER 8 OF 19 WPIX COPYRIGHT 2011   THOMSON REUTERS on STN
AN   2003-755801 [200371]   WPIX Full-text
CR   2004-387384
TI   Manufacture of top-metal fuse structure, comprises forming composite metal layer with second metal layer between upper and lower first metal layers, patterning upper first metal layer, and patterning second and lower first metal layers
DC   L03; U11; U12
IN   CHUANG H
PA   (TSMC-C) TAIWAN SEMICONDUCTOR MFG CO; (TSMC-C) TAIWAN SEMICONDUCTOR MFG CO LTD
CYC 2
PI   US 20030153173 A1 20030814 (200371)* EN 9[4]
     US 6638796   B2 20031028 (200372) EN
     SG 104355   A1 20040621 (200444) EN
ADT US 20030153173 A1 US 2002-75806 20020213; SG 104355 A1 SG 2003-50 20030109
PRAI US 2002-75806   20020213
AB   US 20030153173 A1   UPAB: 20080523

NOVELTY - A top-metal fuse structure is formed by:

(i) providing a structure with an intermetal dielectric layer, a fuse region and a re-distributed layer/bump/bonding pad region;

(ii) forming a composite metal layer comprising a second metal layer between upper and lower first metal layers;

(iii) patterning upper first metal layer; and

(iv) patterning second metal layer and lower first metal layer.

DETAILED DESCRIPTION - Formation of a top-metal fuse structure (10), comprises:

(a) providing a structure having an intermetal dielectric layer (12) formed on it, the structure including a fuse region and a re-distributed layer (RDL)/bump/bonding pad region;

(b) forming a composite metal layer over the intermetal dielectric layer, the composite metal layer includes a second metal layer sandwiched between upper and lower first metal layers;

(c) patterning the upper first metal layer to form an upper metal layer portion within the RDL/bump/bonding pad region; and

(d) patterning the second metal layer and a lower first metal layer.

Within the RDL/bump/bonding pad region (26) to form an RDL/bump/bonding pad; the RDL/bump/bonding pad (30) having a patterned second metal layer portion/lower first metal portion with a width greater than that of the upper metal layer portion and forming a step profile. Within the fuse region to form the top-metal fuse structure.

An INDEPENDENT CLAIM is included for a top-metal fuse structure and RDL/bump/bonding pad structure, comprising:

(1) a structure having an overlying intermetal dielectric layer, including a fuse region and an RDL/bump/bonding pad region;

(2) a top-metal fuse structure over the intermetal dielectric layer within the fuse region, comprising a patterned lower first metal fuse portion over the intermediate dielectric layer , and a patterned second metal layer fuse portion centered over the lower first metal layer fuse portion, the patterned lower first and second metal layers have equal widths; and

(3) a RDL/bump/bonding pad structure over the intermetal dielectric layer within the RDL/bump/bonding region, comprising a patterned lower first metal layer non-fuse portion over the intermetal dielectric layer, having a first width, a patterned second metal layer non-fuse portion centered over the lower first metal layer non-fuse portion, the patterned second metal layer non-fuse portion having a second lower width equal to the first width of the patterned lower first metal layer non-fuse portion and a second upper width less than the first width of the patterned lower first metal layer non-fuse portion, and a patterned upper first metal layer non-fuse portion centered over the patterned second layer non-fuse portion, the patterned upper first metal layer non-fuse portion has a third width less than the second lower width of the patterned second metal layer non-fuse portion, where a step profile is formed at least between the patterned upper first metal layer non-fuse portion, and the patterned second metal layer lower width non-fuse portion.

USE - For forming a top-metal fuse structure.

ADVANTAGE - The method is an improved method of forming a top-metal fuse.

DESCRIPTION OF DRAWINGS - The figure schematically illustrates the method.

Top-metal fuse structure (10)
Intermetal dielectric layer (12)
Barrier layer (15)
Titanium layer (16')
Aluminum layer portions (22')
RDL/bump/bonding pad region (26)
RDL/bump/bonding pad (30)

TECH ELECTRONICS - Preferred Method: The first and second metal layer are patterned using an etching process comprising reactive ion etching (REI) etch process, an RIE end-point detection etch process, or a wet chemical etch process, preferably RIE end-point detection etching process. The upper first metal layer is patterned using an overlying patterned photoresist layer. The upper first metal layer is patterned using an overlying patterned photoresist layer. The second metal layer and the lower first layer are patterned using an overlying patterned photoresist layer.

The method further comprises forming a barrier layer (15) on the intermetal dielectric layer.

Preferred Component: The structure is a substrate comprising a silicon substrate, a silicon-on-oxide substrate, or a gallium arsenide substrate, preferably silicon substrate. The intermetal layer comprises undoped silicate glass (USG), phosphorus silicate glass (PSG), borophosphosilicate glass (BPSG), fluorosilicate glass (FSG), or silicon nitride, preferably USG. The composite metal layer further comprises

third metal layers interposed between the second metal layer and the respective lower and upper first metal layers.
Preferred Condition: The intermetal dielectric layer has a thickness of 3000-15000 Angstrom . The second layer has a thickness of 200-2000, preferably 1000 Angstrom . The upper first metal layer has a thickness of greater than 3000, preferably 8000 Angstrom . The lower first metal layers has a thickness of 2000-10000, preferably 5000 Angstrom . The third metal layer has a thickness of 30-300, preferably 100 Angstrom . The barrier layer has a thickness of 100-800 Angstrom .
INORGANIC CHEMISTRY - Preferred Material: The second metal layer comprises a material comprising titanium nitride, titanium, tantalum nitride, or tantalum, preferably titanium nitride. The upper and lower first metal layers comprise a material comprising aluminum, aluminum copper alloy, copper, or copper alloy, preferably aluminum. The third metal layers comprise titanium, titanium nitride, tantalum, or tantalum nitride, preferably titanium. The barrier layer comprises titanium/titanium nitrides or tantalum/tantalum nitride.

FS CPI; EPI
MC CPI: L03-B04D
EPI: U11-C05G2A; U12-C04
TT TT: MANUFACTURE TOP METAL FUSE STRUCTURE COMPRISE FORMING COMPOSITE LAYER SECOND UPPER LOWER FIRST PATTERN

L133 ANSWER 9 OF 19 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
AN 2002-648993 [200270] WPIX Full-text
DNC C2002-183290 [200270]
DNN N2002-513606 [200270]
TI Semiconductor device production involves etching polycrystalline silicon layer using pattern of silicon oxide film as mask and selectively removing silicon oxide film
DC L03; U11
IN MATSUTANI T
PA (MATU-C) MATSUSHITA DENKI SANGYO KK
CYC 1
PI JP 2002217414 A 20020802 (200270)* JA 12[4]
ADT JP 2002217414 A JP 2001-12585 20010122
PRAI JP 2001-12585 20010122
AB JP 2002217414 A UPAB: 20050527
NOVELTY - A silicon oxide film (14) doped with boron or phosphorus, and a gate insulating film and a polycrystalline silicon film are sequentially laminated on a semiconductor substrate. The polycrystalline silicon film is etched using the pattern of the silicon oxide film as a mask and the silicon oxide film is removed selectively.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a semiconductor device.
USE - For manufacturing a semiconductor device, e.g. a transistor.
ADVANTAGE - Provides a gate electrode structure with high precision and realizes high current drive capability and low resistance.
DESCRIPTION OF DRAWINGS - The figure shows a sectional view of the processes in the manufacture of a semiconductor device. (Drawing includes non-English language text).
Silicon oxide film (14)

FS CPI; EPI
MC CPI: L03-G04A; L04-C02; L04-C07; L04-C11C1; L04-C12A; L04-C12B; L04-E01
EPI: U11-C04D; U11-C05F1; U11-C07C1; U11-C07D1; U11-C18A3
TT TT: SEMICONDUCTOR DEVICE PRODUCE ETCH POLYCRYSTALLINE SILICON LAYER PATTERN OXIDE FILM MASK SELECT REMOVE

L133 ANSWER 10 OF 19 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
AN 2002-089214 [200212] WPIX Full-text
DNC C2002-027406 [200212]
DNN N2002-065745 [200212]
TI Fabrication of a cup-shaped capacitor of a dynamic random access memory (DRAM) cell by deposition of a number of dielectric layers and polysilicon layers interspersed with etching processes
DC L03; U11; U12
IN CHENG J; HSIEH M; JEN T; JENG J; JIAN T; SHIE M; WANG S
PA (CHEN-I) CHENG J; (HSIE-I) HSIEH M; (JENT-I) JEN T; (WANG-I) WANG S; (NYAN-C) NANYA TECHNOLOGY CORP
CYC 2
PI US 20010036700 A1 20011101 (200212)* EN 11[7]
US 6403418 B2 20020611 (200244) EN
TW 463288 A 20011111 (200248) ZH
ADT US 20010036700 A1 Cont of US 1998-6500 19980114; US 20010036700 A1 US 2000-551535 20000418; TW 463288 A TW 1997-106703 19970729; US 6403418 B2 Cont of US 1998-6300 19980114; US 6403418 B2 US 2000-551535 20000418
PRAI TW 1997-106703 19970729
AB US 20010036700 A1 UPAB: 20050524

NOVELTY - Process comprises:

(a) forming isolation regions and MOSFET structures on a silicon substrate (10);

(b) continuously forming 1st and 2nd dielectric layers (20,22) on the substrate surface;

(c) partially etching to open cell contact windows for the MOSFET source regions;

(d) forming a 1st polysilicon layer (30) on the 2nd dielectric layer and filling into the cell contact windows;

(e) forming a 3rd dielectric layer and defining 3rd dielectric crowns;

(f) depositing a 2nd polysilicon layer (34A);

(g) anisotropically etching the 2nd polysilicon layer to form the storage node of the capacitor;

(h) removing the 3rd dielectric crowns (32A);

(i) forming a capacitor dielectric layer overlying the storage node of the capacitor; and

(j) forming a 3rd polysilicon layer over the capacitor dielectric layer as the top electrode.

DETAILED DESCRIPTION - A further process similar to the above is INDEPENDENTLY CLAIMED.

USE - Capacitor fabrication for high density DRAMS.

ADVANTAGE - The cells have greater capacitance per unit area and can be produced with reduced processing steps and cost.

DESCRIPTION OF DRAWINGS - The diagram shows a cross-section of a DRAM cell after the 3rd dielectric crown is removed.

Semiconductor substrate (10)
Field oxide region (12)
Gates (14)
Pad oxides (16)
Source/drain region (18)
1st dielectric layer (20)
2nd dielectric layer (22)
Spacers (28)
1st polysilicon layer (30A)
Dielectric crowns (32A)
2nd polysilicon layer (34A)

TECH INORGANIC CHEMISTRY - Preferred Dielectric Layers: The 1st layer is made of borophosphosilicate glass (BPSG), natural silicate glass (NSG) or tetraethylorthosilicate (TEOS). The 2nd layer is made of silicon nitride or silicon oxynitride and has thickness of 200-1,000 Angstroms. The 3rd layer is made of BPSG, NSG phosphosilicate glass (PSG) and spin on glass (SOG), and has a thickness of 4,000-10,000 Angstroms. The capacitor dielectric layer is selected from a nitride/oxide double layer, an oxide/nitride/oxide triple layer and tantalum oxide, and has a thickness of 1,000-2,000 Angstroms.

FS CPI; EPI

MC CPI: L03-G04A; L04-C10B; L04-C12C; L04-C14A
EPI: U11-C01J1; U11-C05G1B; U11-C18B5; U12-C02A1

TT TT: FABRICATE CUP SHAPE CAPACITOR DYNAMIC RANDOM ACCESS MEMORY DRAM CELL DEPOSIT NUMBER DIELECTRIC LAYER INTERSPERSED ETCH PROCESS

L133 ANSWER 11 OF 19 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN

AN 1999-347832 [199929] WPIX Full-text

CR 2000-441904

TI Stack and trench capacitor formation by chemical mechanical polishing of ferroelectric random access memory capacitor

DC G06; L03; U11; U12; U13; U14

IN BAUM T H; KIRLIN P S; VAN BUSKIRK P C; XU C; VANBUSKIRK P C

PA (ATMI-C) ADVANCED TECHNOLOGY MATERIALS

CYC 79

PI

WO 9927581	A1	19990603	(199929)*	EN	49[16]
AU 9915893	A	19990615	(199944)	EN	
US 5976928	A	19991102	(199953)	EN	
EP 1040518	A1	20001004	(200050)	EN	
KR 2001032312	A	20010416	(200163)	KO	
JP 2001524755	T	20011204	(200203)	JA	42
KR 643061	B1	20061110	(200757)	KO	

ADT WO 9927581 A1 WO 1998-US24569 19981117; US 5976928 A US 1997-975366 19971120; EP 1040518 A1 EP 1998-960248 19981117; EP 1040518 A1 WO 1998-US24569 19981117; JP 2001524755 T WO 1998-US24569 19981117; AU 9915893 A AU 1999-15893 19981117; JP 2001524755 T JP 2000-522624 19981117; KR 2001032312 A KR 2000-705522 20000520; KR 643061 B1 WO 1998-US24569 19981117; KR 643061 B1 KR

2000-705522 20000520
FDT AU 9915893 A Based on WO 9927581 A; EP 1040518 A1 Based on WO 9927581 A; JP 2001524755 T Based on WO 9927581 A; KR 643061 B1 Previous Publ KR 2001032312 A; KR 643061 B1 Based on WO 9927581 A
PRAI US 1997-975366 19971120
AB WO 1999027581 A1 UPAB: 20091214

NOVELTY - A ferroelectric capacitor structure is formed by sequentially depositing a bottom electrode layer, a ferroelectric layer and a top electrode layer on a base structure, then planarizing the obtained capacitor precursor structure by chemical mechanical polishing (CMP).

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for (1) the fabrication of a stack capacitor on a substrate including buried circuitry overlaid by an isolation dielectric, by forming a via in the isolation dielectric to the buried circuitry, depositing a plug in the via, planarizing the isolation dielectric and plug, depositing isolation dielectric, forming a capacitor recess in the isolation dielectric surface, depositing a bottom electrode layer, a ferroelectric layer and a top electrode layer, optionally with a conductive barrier between the isolation dielectric and bottom electrode and optionally with a dielectric buffer over the top electrode, followed by planarizing, depositing an insulation passivation layer and interlevel dielectric, forming a via in this barrier structure, depositing a diffusion barrier layer and metallization layer to fill the via, and patterning the metallization to form a line structure; and (2) the fabrication of a trench capacitor by forming a capacitor recess in a substrate, depositing a bottom electrode layer, a ferroelectric layer and a top electrode layer, optionally with a conductive barrier between the isolation dielectric and bottom electrode and optionally with a dielectric buffer over the top electrode, followed by planarizing, depositing an insulation passivation layer and interlevel dielectric to form a barrier layer, forming a via, depositing a diffusion barrier layer and patterning, forming a first via to a device region of the substrate, forming circuitry including a plate and a first line element of a word and a bit line structure, depositing an isolation dielectric, forming a second via to a device region of the substrate, metallizing to fill the via and then patterning to form a complimentary line element of the word and a bit line structure.

USE - In advanced DRAMs and ferroelectric RAMs (FeRAMS).

ADVANTAGE - Capacitor geometries are only limited by the resolution of the lithography and the conformality of the thin film deposition process, so that 0.18 or 0.12 mum structures are possible without dry etching the noble metals or ferroelectric layer. The capacitors have significant contribution of sidewall area, without the need for separate patterning of top and bottom electrodes. The plug-barrier-bottom electrode interface is protected from exposure to oxidation.

DESCRIPTION OF DRAWINGS - The drawing shows a stack capacitor produced by the above process.

Top electrode (34)
Interlevel dielectric (38)
Via (40)
Diffusion barrier (42)

TECH INORGANIC CHEMISTRY - Preferred Materials: The substrate is Si or GaAs. A buffer layer is formed over the capacitor

precursor structure before CMP. Dry etching of the electrode layers or ferroelectric layer does not occur. The ferroelectric capacitor has a feature size below 0.35 mum. The isolation and interlevel dielectric are SiO2, Si3N4, B-doped SiO2,
P-doped SiO2, B- and P
-doped SiO2, low dielectric organic insulator,
SiOxFy, B-doped SiOxFy, P-doped SiOxFy
or B- and P-doped SiOxFy, where x+y = 2.
The via and capacitor recess are formed by photolithography and dry etching. The plug is Si doped with B, P, and or As, or W. Planarization is by dry etching or CMP. The top of the plug is cleaned by sputter etching and heat treating prior to depositing the conductive barrier layer. The conductive barrier layer is TaWN, TaN, TiWN, TaSiN, TaAlN, NbN, TaTiN, TiN, TiSiN, TiAlN, IrO2 or SiC. The bottom and top electrodes are noble metal, noble metal/non-noble metal alloy, noble metal/noble metal oxide mixtures, noble metal multilayers or noble metal/non-noble metal multilayers
, formed by sputtering or CVD. The ferroelectric layer is PZT, SBT, Bi titanate, BST, LaCaMnO3, or materials formed by (non) covalent substitutions in these materials.
CMP involves using a slurry of silica, alumina or ceria abrasives, together with additives. Multiple CMP steps may be carried out using different slurry materials. After planarizing, conductive residue is removed by a dry or wet etch. Post CMP annealing is used to remove physical and/or chemical damage to the ferroelectric layer. The insulation passivation layer is TiO2, HfO2, Nb2O5, ZrO2, Ta2O5, Si3N4 or their mixtures. The metallization is W, Al, Cu or Al-Cu alloy. The metallization is patterned by photolithography and dry etching or by a (dual) damascene process. The circuitry is at least in part polysilicon.

FS CPI; EPI

MC CPI: G06-D06; G06-E; G06-E04; L03-G04A; L04-C11C; L04-C14A; L04-C26
EPI: U11-C05G1B; U11-C06A1A; U12-C02A1; U12-C02F; U13-C04B1A; U14-A03B4; U14-A03F

TT TT: STACK TRENCH CAPACITOR FORMATION CHEMICAL MECHANICAL POLISH FERROELECTRIC RANDOM ACCESS MEMORY

L133 ANSWER 12 OF 19 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN

AN 1998-363054 [199831] WPIX Full-text

DNC C1998-111787 [199831]

DNN N1998-283432 [199831]

TI Forming insulating layer in semiconductor device with dielectric layer - comprises heating substrate with silicon surface, and passing over nitric oxide and nitrous oxide gas

DC L03; U11

IN KWONG D; LEONARDUZZI G D

PA (SCOT-N) SCOTT SPECIALTY GASES INC

CYC 76

PI WO 9827580 A1 19980625 (199831)* EN 25[6]
AU 9854299 A 19980715 (199846) EN

ADT WO 9827580 A1 WO 1997-US20175 19971103; AU 9854299 A AU 1998-54299 19971103

FDT AU 9854299 A Based on WO 9827580 A
PRAI US 1996-753864 19961203
AB WO 1998027580 A1 UPAB: 20050521

Forming an insulating layer in a semiconductor device, comprises placing a substrate having a silicon (Si) surface into a chamber and heating it to at least 750°C. Gaseous nitric oxide (NO) and nitrous oxide (N2O) are passed into the chamber and over the heated substrate. The gases are in contact with the heated Si surface for sufficient time to form a layer of silicon oxide (SiO2) having nitrogen distributed therein.

Also claimed is a method of forming an insulated layer in a semiconductor device where the gaseous mixture has 50-95 vol.% N2O and 5-50 vol.% NO.

USE - Used in the fabrication of semiconductor devices having an oxynitride dielectric layer between the gate and the channel. The oxynitride dielectric layer has a varying nitrogen distribution, with a peak concentration near to the gate. The semiconductor is used in a MOS device (all claimed). Also used to make semiconductors with gate dimensions < 0.25 µm.

ADVANTAGE - The process results in an oxynitride dielectric layer with multiple identifiable regions with different nitrogen concentrations.

ABDT WO9827580

Forming an insulating layer in a semiconductor device, comprises placing a substrate having a silicon (Si) surface into a chamber and heating it to at least 750°C. Gaseous nitric oxide (NO) and nitrous oxide (N2O) are passed into the chamber and over the heated substrate. The gases are in contact with the heated Si surface for sufficient time to form a layer of silicon oxide (SiO2) having nitrogen distributed therein.

Also claimed is a method of forming an insulated layer in a semiconductor device where the gaseous mixture has 50-95 vol.% N2O and 5-50 vol.% NO.

USE

Used in the fabrication of semiconductor devices having an oxynitride dielectric layer between the gate and the channel. The oxynitride dielectric layer has a varying nitrogen distribution, with a peak concentration near to the gate. The semiconductor is used in a MOS device (all claimed). Also used to make semiconductors with gate dimensions < 0.25 µm.

ADVANTAGE

The process results in an oxynitride dielectric layer with multiple identifiable regions with different nitrogen concentrations.

PREFERRED METHOD

The NO and N2O are supplied at a ratio of 5-9:9-20, at a flow rate of 1000-104 SCCM. The Si surface is heated at 750-1100°C, by rapid infrared heating or in a furnace. The gases are maintained in contact with the silicon surface for 30 seconds to 2 minutes.

PREFERRED DESIGN

A p + and/or boron doped gate is formed on the SiO2 layer. A channel is formed below the SiO2 layer.

The interfacial region forms a barrier against charge carriers travelling in the channel. The top region forms a barrier against boron diffusion from the electrode. The semiconductor device has a thickness < 1 μm. The treated SiO2 is a gate dielectric. The SiO2 has an interfacial region on the Si surface, a bulk region and a top region with a greater concentration of nitrogen. The substrate is a Si wafer.
(RB)

FS CPI; EPI
MC CPI: L04-C12A
EPI: U11-C05B1; U11-C05B7
TT TT: FORMING INSULATE LAYER SEMICONDUCTOR DEVICE DIELECTRIC COMPRISE HEAT SUBSTRATE SILICON SURFACE PASS NITRIC OXIDE NITROUS GAS
AW: OXY NITRIDE

L133 ANSWER 13 OF 19 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
AN 1997-153587 [199714] WPIX Full-text
CR 2001-289754
TI Mfg. insulator structure for poly:silicon@ resistors in IC - by forming glass insulating layer on substrate followed by poly:silicon@ resistor and PECVD silica insulating layer
DC L03; U11
IN LEE C
PA (TSMC-C) TAIWAN SEMICONDUCTOR MFG CO LTD
CYC 1
PI US 5605859 A 19970225 (199714)* EN 8[1]
ADT US 5605859 A US 1995-498355 19950705
PRAI US 1995-498355 19950705
AB US 5605859 A UPAB: 20050519
A method of forming a poly-Si resistor structure within an IC comprises forming a glassy insulating layer (20) directly on a semiconductor substrate (10), forming a poly-Si resistor layer (19) on this and then a second insulating layer of silica (21), formed by PECVD of silane at 300-500°C and 5000-10,000Å per minute, and having a refractive index of 1.4-1.5.
USE - As poly-Si resistors in ICs such as DRAMs, SRAMs, FETs and bipolar transistors
ADVANTAGE - Changes in resistance caused by subsequent processing are minimised and the structure is readily formed in existing IC mfg. processes.
ABDT US5605859
A method of forming a poly-Si resistor structure within an IC comprises forming a glassy insulating layer (20) directly on a semiconductor substrate (10), forming a poly-Si resistor layer (19) on this and then a second insulating layer of silica (21), formed by PECVD of silane at 300-500°C and 5000-10,000Å per minute, and having a refractive index of 1.4-1.5.
USE
As poly-Si resistors in ICs such as DRAMs, SRAMs, FETs and bipolar transistors
ADVANTAGE
Changes in resistance caused by subsequent processing are minimised

and the structure is readily formed in existing IC mfg. processes.
PREFERRED METHOD
The first insulating layer is 6000-9000Å thick, is of BSG, PSG, or BPSG and contains 2-3 wt.% B and 3-4 wt.% P.
The resistor is 500-1000Å thick and is doped. There is a third insulating layer on the second which comprises three insulating layers in a sandwich, the top and bottom being formed by PECVD using TEOS and oxygen and the middle by sub-atmos. CVD using TEOS and ozone. These three layers are 1000-3000Å, 3000-6000Å and 1000-3000Å respectively. (RP)

FS CPI; EPI
MC CPI: L04-C10B; L04-C12A; L04-C12D; L04-E
EPI: U11-C05B9A; U11-C05G1A
TT TT: MANUFACTURE INSULATE STRUCTURE POLY SILICON@ RESISTOR IC FORMING GLASS LAYER SUBSTRATE FOLLOW SILICA

L133 ANSWER 14 OF 19 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
AN 1996-479020 [199648] WPIX Full-text
DNC C1996-149603 [199648]
DNN N1996-403975 [199648]
TI Semiconductor memory device having stacked capacitor structure - where capacitor is formed by selectively removing silicon oxide layer contg. boron and/or phosphorus impurities using chemical soln. etch
DC L03; U11; U12; U13; U14
IN FUJIWARA H; FUJIWARA S; HIROTA T
PA (NIDE-C) NEC CORP
CYC 3

PI	EP 740339	A2 19961030	(199648)*	EN	14[3]
	JP 08306876	A 19961122	(199706)	JA	8[13]
	US 6300186	B1 20011009	(200162)	EN	
	EP 740339	B1 20030326	(200323)	EN	
	DE 69626881	E 20030430	(200336)	DE	

ADT EP 740339 A2 EP 1996-106454 19960424; JP 08306876 A JP 1995-103760 19950427; DE 69626881 E DE 1996-69626881 19960424; DE 69626881 E EP 1996-106454 19960424; US 6300186 B1 US 1996-637038 19960424
FDT DE 69626881 E Based on EP 740339 A
PRAI JP 1995-103760 19950427
AB EP 740339 A2 UPAB: 20050702
Mfr. of semiconductor device having a MOS transistor formed on a Si substrate (1) is claimed. A stacked capacitor constituted by an information-storage electrode is provided above the MOS transistor through as insulating interlayer (6). A counter-electrode (12) is separate from an information-storage electrode (8b,10) due to a capacitor insulating film (11). The method includes: a) adding an impurity in a Si oxide film (9) which is formed on the insulating interlayer and used to shape the information-storage electrode; and b) selectively etching the Si oxide-film using a soln. contg. phosphoric acid, sulphuric acid and/or nitric acid, or a soln. contg. a mixture of liq. ammonia soln. and H_2O_2 soln., thereby forming the capacitor.

USE - Useful in the field of semiconductor integrated circuit mfr., esp. for fabricating a three-dimensional capacitor electrode of a memory device, e.g. a DRAM.

ADVANTAGE - Allows the formation of capacitor electrodes having fin-like structures and/or cylindrical structures, without the need for a SiN film to prevent etching of the insulating interlayer .

ABDT EP740339

Mfr. of semiconductor device having a MOS transistor formed on a Si substrate (1) is claimed. A stacked capacitor constituted by an information-storage electrode is provided above the MOS transistor through as insulating interlayer (6). A counter-electrode (12) is separate from an information-storage electrode (8b,10) due to a capacitor insulating film (11).

The method includes:

a) adding an impurity in a Si oxide film (9) which is formed on the insulating interlayer and used to shape the information-storage electrode; and

b) selectively etching the Si oxide-film using a soln. contg. phosphoric acid, sulphuric acid and/or nitric acid, or a soln. contg. a mixture of liq. ammonia soln. and H2O2 soln., thereby forming the capacitor.

USE

Useful in the field of semiconductor integrated circuit mfr., esp. for fabricating a three-dimensional capacitor electrode of a memory device, e.g. a DRAM.

ADVANTAGE

Allows the formation of capacitor electrodes having fin-like structures and/or cylindrical structures, without the need for a SiN film to prevent etching of the insulating interlayer.

PREFERRED METHOD

The insulating interlayer in a Si oxide film contg. no impurity. The Si oxide film contg. the impurity comprises a silicate glass contg. boron and/or phosphorus. The impurity-doped Si oxide film may contain alternate layers of two types of Si oxide films in a multilayer structure. The information-storage electrode uses a thin Si film contg. As or P impurity, the As and P impurities may be introduced into the information-storage electrode after the step of selectively etching the impurity-doped Si oxide layer. (RP)

FS CPI; EPI

MC CPI: L03-G04A; L04-C07; L04-C07C; L04-C11C; L04-C12A; L04-C14A; L04-E01B

EPI: U11-C05F6; U11-C05G1B; U12-C02A1; U13-D03A; U14-A03B4

TT TT: SEMICONDUCTOR MEMORY DEVICE STACK CAPACITOR STRUCTURE FORMING SELECT REMOVE SILICON OXIDE LAYER CONTAIN BORON PHOSPHORUS IMPURE CHEMICAL SOLUTION ETCH

L133 ANSWER 15 OF 19 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN

AN 1996-424672 [199642] WPIX Full-text

TI Forming a contact to doped silicon in VLSI - comprises forming semiconductor devices within a semiconductor wafer

, forming a layer of silica and of glass and reflowing and etching anisotropically, preventing BPSG flow at contact open top, etc.

DC L03; U11
IN LEE J; LIAW J; TENG M
PA (TSMC-C) TAIWAN SEMICONDUCTOR MFG CO LTD
CYC 1
PI US 5554565 A 19960910 (199642)* EN 9[2]
ADT US 5554565 A US 1996-606832 19960226
PRAI US 1996-606832 19960226
IPCR H01L0021-70 [I,C]; H01L0021-768 [I,A]
EPC H01L0021-768B; H01L0021-768C4
AB US 5554565 A UPAB: 20060111

A method of forming a contact to a Si semiconductor device and connecting to a metallic interconnection network comprises forming semiconductor devices within a semiconductor wafer (10), forming a layer of silica and then of glass (18) and reflowing and etching anisotropically. A second silica is formed to give a dielectric sandwich, photoresist patterned and etched to give vertically walled contact openings in the sandwich and dopant implanted. Photoresist is removed, the dopant activated by RTA, a Ti layer (26) formed over the wafer and a barrier layer formed. A second RTA is performed and a W layer deposited and etched to form W plugs (30).
Also claimed is a method as above for forming contacts to Si devices having both p- and n-diffusions on the same substrate in which patterning exposes p- and n-contact openings separately.

USE - Used in forming metal-to-silicon contacts in VLSI.

ADVANTAGE - BPSG flow at the top of the contact openings is prevented, higher annealing temps. are possible and contact resistance is reduced.

ABDT US5554565

A method of forming a contact to a Si semiconductor device and connecting to a metallic interconnection network comprises forming semiconductor devices within a semiconductor wafer (10), forming a layer of silica and then of glass (18) and reflowing and etching anisotropically. A second silica is formed to give a dielectric sandwich, photoresist patterned and etched to give vertically walled contact openings in the sandwich and dopant implanted. Photoresist is removed, the dopant activated by RTA, a Ti layer (26) formed over the wafer and a barrier layer formed. A second RTA is performed and a W layer deposited and etched to form W plugs (30).
Also claimed is a method as above for forming contacts to Si devices having both p- and n-diffusions on the same substrate in which patterning exposes p- and n-contact openings separately.
USE
Used in forming metal-to-silicon contacts in VLSI.
ADVANTAGE
BPSG flow at the top of the contact openings is prevented, higher annealing temps. are possible and contact resistance is reduced.

PREFERRED METHOD

The wafer is p with P dopant or n with BF 2+ dopant, the first silica layer is deposited from TEOS at 300-700 ° C and is 1000-2000 A

thick,m the glass i BPSG or PSG and is 5000-15000
A thick and the second silica is 1000-3000 A thick and deposited by PECVD from TEOS or a silane/O 2 or N 2 O mixt. at 300-700 ° C. The glass is flowed at 800-900 ° C. Unidirectional etching is RIE using CF 4 , the glass is etched back to 4000-7000 A thick, the Ti layer is 300-800 A thick and the barrier layer is TiN and is 800-2000 A thick, of TiW 800-2000 A thick. Both RTA steps are under nitrogen using a halogen lamp for 20-30 s. and are at 900-1000 and 600-700 ° C respectively. W is deposited from WF 6 and H 2 at 415-500 ° C in a cold-walled low-temp. CVD system. First doping is at 1-2E15 cm - 2 and 30-100 keV for P and 2-5E14 cm - 2 and 30-100 keV for B.

FS CPI; EPI
MC CPI: L04-C11; L04-C13B
EPI: U11-C05E1; U11-C05G2C; U11-D03B2
TT TT: FORMING CONTACT DOPE SILICON VLSI COMPRISE SEMICONDUCTOR DEVICE WAFER LAYER SILICA GLASS REFLOW ETCH ANISOTROPE PREVENT BPSG FLOW OPEN TOP

L133 ANSWER 16 OF 19 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
AN 1992-235799 [199229] WPIX Full-text
DNC C1992-106309 [199321]
DNN N1992-179544 [199321]
TI Etching laminated substrate esp. in planarising process - includes detecting interface by sensing change in compsn. of etching gas plasma
DC A85; L03; U11
IN SATO F; SATOU F
PA (NIDE-C) NEC CORP
CYC 5

PI						
	EP 494745	A2	19920715	(199229)*	EN	9[3]
	US 5272115	A	19931221	(199351)	EN	7[2]
	JP 06045327	A	19940218	(199412)	JA	5[4]
	EP 494745	A3	19940316	(199520)	EN	
	EP 494745	B1	19991103	(199951)	EN	
	DE 69230229	E	19991209	(200004)	DE	

ADT EP 494745 A2 EP 1992-300080 19920106; JP 06045327 A JP 1991-795 19910109; US 5272115 A US 1991-816035 19911230 ; DE 69230229 E DE 1992-69230229 19920106; EP 494745 A3 EP 1992-300080 19920106; EP 494745 B1 EP 1992-300080 19920106; DE 69230229 E EP 1992-300080 19920106
FDT DE 69230229 E Based on EP 494745 A
PRAI JP 1991-795 19910109
AB EP 494745 A2 UPAB: 20050504

Surface of a semiconductor laminate comprising different upper and lower layers etched by: ion etching the upper layer in a gas plasma; detecting exposure of the lower layer by sensing a sudden change in the concn. of a constituent in the plasma; and controlling the etching in response. The constituent is pref. reaction prod. of the material of the lower layer and an orginal constituent of the plasma gas. Planarisation is achieved by: coating a semiconductor wiring substrate with different first and second insulating films and an upper coating layer; and ion etching, as above, the

upper coating layer until the second insulating film is exposed, and then the second insulating layer until the first insulating layer is exposed, so that the surface is planarised. Remaining parts of the coating layer are then removed and an insulating layer is added on the second insulating film and exposed parts of the first insulating layer.

USE/ADVANTAGE - Esp. in planarising surfaces wiring substrate surfaces. Close etching control is obtd..

FS   CPI; EPI
MC   CPI: A12-E07C; L04-C07A
     EPI: U11-C05B9; U11-C05D1; U11-C07A1; U11-C07C3; U11-C07D3
TT   TT: ETCH LAMINATE SUBSTRATE PLANAR PROCESS DETECT INTERFACE
         SENSE CHANGE COMPOSITION GAS PLASMA

L133 ANSWER 17 OF 19 WPIX COPYRIGHT 2011   THOMSON REUTERS on STN
AN   1988-243769 [198835]   WPIX Full-text
DNC C1988-108950 [199321]
DNN N1988-185460 [199321]
TI   Ultraviolet erasable semiconductor memory device - contains both PSG and boron PSG regions and combines transparency with lower temp. processing
DC   L03; U11; U14
IN   MORI S
PA   (TOKE-C) TOSHIBA KK
CYC 4

PI	EP 280276	A	19880831	(198835)*	EN	11[5]
	JP 63211766	A	19880902	(198841)	JA	
	JP 01017477	A	19890120	(198909)	JA	
	US 4847667	A	19890711	(198935)	EN	9
	EP 280276	B1	19930519	(199320)	EN	16[5]
	JP 05029150	B	19930428	(199320)	JA	5
	DE 3881074	G	19930624	(199326)	DE	

ADT EP 280276 A EP 1988-102739 19880224; JP 63211766 A JP 1987-42925 19870227; JP 01017477 A JP 1987-42925 19870227; JP 05029150 B JP 1987-42925 19870227; JP 63211766 A JP 1987-174111 19870713; JP 01017477 A JP 1987-174111 19870713; DE 3881074 G DE 1988-3881074 19880224; EP 280276 B1 EP 1988-102739 19880224; DE 3881074 G EP 1988-102739 19880224; US 4847667 A US 1988-159963 19880224
FDT DE 3881074 G Based on EP 280276 A; JP 05029150 B Based on JP 63211766 A
PRAI JP 1987-174111   19870713
     JP 1987-42925   19870227
AB   EP 280276 A   UPAB: 20050429

An ultraviolet erasable nonvolatile semiconductor memory device has at least one memory element (11-1) of stacked gate structure on a doped semiconductor substrate (12) with a thermal oxide film (17) around it and a P doped silica film (19) above this. In the concave portions of this film (19) corresponding to the side of the stacked gate is a P and B doped silica film (20). The memory element (11-1) includes doped regions (18-1 and 18-2) of opposite type to the substrate (12) and floating gate (14-1) and control gate (16-1), both enclosed with insulating films of SiO_2 and Si_3N_4/SiO_2

laminate. The above gate regions (14-1, 16-1) are composed of polysilicon or refractory metals or their silicides. Doping levels in the P doped silica film (19) and the B and P doped film (20) exceeed 10 18 cm power (-3). Also claimed is a method of manufacturing the above memory device which contains a heat treatment stage below 900 deg.C, in which the B and P doped oxide film (20) -BPSG- melts and fills the concave portion of the surface (19).

ADVANTAGE - In existing processes the advantage of using BPSG film to give lower temperature planarisation is offset by its lower UV transparency with consequent reduction in data erasing speed. The new process overcomes this difficulty by using PSG-only regions where transparency is required and BPSG in the planarisation regions.

FS CPI; EPI
MC CPI: L03-G04A; L04-E
EPI: U11-C05B7; U14-A06C
TT TT: ULTRAVIOLET ERASE SEMICONDUCTOR MEMORY DEVICE CONTAIN PSG BORON REGION COMBINATION TRANSPARENT LOWER TEMPERATURE PROCESS
AW: PHOSPHORUS SILICON

L133 ANSWER 18 OF 19 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
AN 1988-159448 [198823] WPIX Full-text
DNC C1988-071407 [199321]
DNN N1988-121599 [199321]
TI Contact stud process for VLSI or ULSI - by etching contact windows through BPSG layer on semiconductor wafer using tri:fluoro:methane-oxygen gas mixt.
DC L03; U11
PA (ANON-C) ANONYMOUS
CYC 1
PI RD 289063 A 19880510 (198823)* EN

ADT RD 289063 A RD 1988-289063 19880420
PRAI RD 1988-289063 19880420
IC IC H01L000-01
AB RD 289063 A UPAB: 20050428
A process for forming contact windows and titanium studs to facilitate metal interconnections in an integrated circuit comprises (1) providing a semiconductor wafer having integrated circuit devices covered by a layer of borophosphosilicate glass (BPSG). (2) depositing a layer of photoresist on the BPSG layer. (3) lithographically defining a contact mask in the photoresist layer. (4) vertically etching the contact windows through the BPSG with a CHF3/O2 gas mixt. in a reactive ion etch chamber, (5) etching the contact windows with a 50:1 buffered hydrofluoric acid soln. (6) evapg. titanium in a conformal manner such that the contact windows are filled. (7) blanket etching the titanium layer until the titanium remains only in the contact windows. (8) depositing the metal interconnect layer.
FS CPI; EPI
MC CPI: L04-C10A; L04-C15
EPI: U11-C05D3; U11-C05D4
TT TT: CONTACT STUD PROCESS VLSI ETCH WINDOW THROUGH BPSG LAYER SEMICONDUCTOR WAFER TRI FLUORO METHANE OXYGEN GAS MIXTURE

AW: SCALE INTEGRATE ULTRA SCALE INTEGRATE BORO
    PHOSPHO SILICATE GLASS

L133 ANSWER 19 OF 19 WPIX COPYRIGHT 2011   THOMSON REUTERS on STN
AN   1986-327038 [198650]   WPIX Full-text
DNC C1986-141547 [199321]
DNN N1986-244030 [199321]
TI   LPCVD of insulating boron-phosphorus-
     silicate glass layer - for VLSI-circuits; uses organic source
     compounds
DC   L03; P42; U11
IN   BECKER F S; PAWLIK D
PA   (SIEI-C) SIEMENS AG
CYC 8
PI   EP 204182   A 19861210 (198650)* DE 5[1]
     JP 61275136   A 19861205 (198703) JA
     US 4791005   A 19881213 (198901) EN
     EP 204182   B 19910605 (199123) EN
     DE 3679596   G 19910711 (199129) DE
ADT EP 204182 A EP 1986-106479 19860513; DE 3679596 G DE
     1985-3518452 19850522; JP 61275136 A JP 1986-112416
     19860516; US 4791005 A US 1987-113412 19871027
PRAI DE 1985-3518452   19850522
AB   EP 204182 A   UPAB: 20050426
     A process for depositing a mixed boron- and phospho -silicate glass-film uses tetra-ethylsilicate, (C2H5O)4Si ot TEOS, trimethylborate, (CH3O)3B or TMB, and trimethylphosphate, (CH3O)3P or TMP. The cpds. are thermally decomposed at a temp. over 600, pref. between 600 and 700 deg.C., in a reactor-tube in counter-flow at a reduced pressure,pref. between 15 and 100 Pa. The source-materials enter the tube separately and are transported by using O2 or N2 to percolate through the TEOS and TMB material held at a temp. between 30 and 60 deg.C and through the TMP material held at a temp. over 60 deg.C. Instead of TMP a mixture of PH3 and O2 with a ration of greater than 0.2 may be used.

     USE/ADVANTAGE - The process allows a better control over the compsn. by using a more stable Boron-source than current technology. The glass-layer formed has a better resistance to moisture. All of the Phosphorus incorporated in the layer contributes to the improvement of flow-conditions during subsequent processing. The method is less sensitive to leaks and the edge-coverage is improved. The process is used for the deposition of intermediate insulating layers in VLSI-processing especially for high density memory-devices.
FS   CPI; GMPI; EPI
MC   CPI: L04-C12D
     EPI: U11-C05B1
TT   TT: INSULATE BORON PHOSPHORUS SILICATE
         GLASS LAYER VLSI CIRCUIT ORGANIC SOURCE COMPOUND
     AW: LOW PRESSURE CHEMICAL VAPOUR DEPOSIT SCALE INTEGRATE

=> D L134 1-36 TI

L134 ANSWER 1 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Light scattering element for optical wave guide, has core and silicon structure of transistor, which are formed from monocrystalline silicon on same substrate and salicide block layer, which is deposited on integrated circuit

L134 ANSWER 2 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Dynamic random access memory construction for forming memory array, comprises agglomerates comprising noble metal(s), including spaced islands which are in direct physical contact with insulative material and conductive layers

L134 ANSWER 3 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Method for forming boro-phospho-silicate glass layer

L134 ANSWER 4 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Formation of contact electrically connected to metal line for semiconductor device, involves forming contact hole in insulation layer, and forming single metal layer having planar top surface upon planar surface of insulation layer

L134 ANSWER 5 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Formation of conductive contact involves depositing metal to form metal plug within opening through metal layer by electroless plating process, and depositing metal onto metal plug by plating process to fill opening in substrate

L134 ANSWER 6 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Deposition of e.g. platinum film on substrate e.g., capacitor for memory cell, involves flowing gaseous platinum group metal precursor into chemical vapor deposition chamber in the presence of oxygen and nitrous oxide mixture

L134 ANSWER 7 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Formation of contact electrically connected to metal line for microelectronic devices, involves forming contact hole in insulation layer provided on semiconductor substrate, forming first and second metal layers, and heating the substrate

L134 ANSWER 8 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Manufacture of semiconductor structure comprises using boron and/or phosphorus-containing liquid compounds, vaporizing, directing gases toward substrate and thermally treating to form boron and/or phosphorus-containing silica layer

L134 ANSWER 9 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Test pad in semiconductor memory, comprises substrate, metal layer, first dielectric layer, plug, aluminum layer, titanium boronitride layer, and second dielectric layer etched to expose titanium boronitride layer

L134 ANSWER 10 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Formation of conductive element in integrated circuit comprises forming semiconductor devices, interconnecting devices to form circuit having circuit nodes, and depositing exposed pad layer in electrical contact with circuit node(s)

L134 ANSWER 11 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Formation of local interconnect for integrated circuitry by etching second dielectric layer selectively relative to first dielectric layer to form local interconnect outline within second dielectric layer to extend between transistors

L134 ANSWER 12 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Formation of uniform nitride dielectric layer on nitride resistive and receptive materials, involves implanting surface-modifying agent to nitride resistive material, and forming nitride dielectric layer

L134 ANSWER 13 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Micromechanical device used for microsensors, includes device substrate, handle substrate, first trench, dielectric, cavity , and second trench

L134 ANSWER 14 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Formation of self-aligned mask layer over substrate for protecting corners of substrate, involves forming mask layer over exposed surface of substrate having etched feature

L134 ANSWER 15 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Silicon nitride layer formation method for fabrication of metal oxide semiconductor field effect transistor gates, involves forming dichlorosilane seeding layer and tetrachlorosilane nitride layer

L134 ANSWER 16 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Microfabricated sensors for monitoring a change in force or membrane surface properties of sensor membrane, has a substrate and one or more layers formed on the substrate

L134 ANSWER 17 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Integrated circuit element formation on semiconductor wafer, involves forming silicon nitride shield layer on dielectric layer, after which conductive material is selectively deposited in cavity in dielectric layer

L134 ANSWER 18 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Etching of insulating oxide layer of semiconductor device involves etching of insulating layer using a fluorocarbon gas followed by etching using hydrogen containing fluorocarbon gas

L134 ANSWER 19 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Platinum group metal deposition for integrated circuit structure, involves depositing metal on substrate in chemical vapor deposition

chamber, in presence of oxygen and nitrous oxide, at preset temperature and pressure

L134 ANSWER 20 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Manufacture of stencil mask by defining opening locations in substrate, providing dopant in substrate, forming openings in opening locations, providing additional dopant, and forming stencil mask

L134 ANSWER 21 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Capacitance-type pressure sensor includes diaphragm fixing portions disposed internally of cavity region so that single sheet of diaphragm is partitioned and regionally allotted to regions of pressure sensor units

L134 ANSWER 22 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI High density metal oxide semiconductor gated device e.g., power metal oxide semiconductor field effect transistor includes a shallow body region underlying a source region contact area

L134 ANSWER 23 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Cavity fuse formation on gate conductor stack, e.g. for use in DRAM circuit manufacture, includes anisotropic and isotropic etching steps

L134 ANSWER 24 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Formation of a contact opening to a semiconductor substrate by using an etch buffer layer that will act as an etch uniformity aid and may add structural utility in the finished microelectronic device

L134 ANSWER 25 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Formation of a cavity to form container cells for semiconductor capacitors used in, e.g. memory circuits, by selecting an etchable material, selecting etching process(es), forming an etchable material layer, and etching

L134 ANSWER 26 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Selective etching of silicon containing material for manufacture of semiconductor devices

L134 ANSWER 27 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Protective film layer arrangement in inkjet recording head for inkjet recorders - protects heat generator consisting of heat resistor with wiring

L134 ANSWER 28 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
TI Mfr. of insulation elements of integrated circuits - includes additional deposition of phosphor or borosilicate glass onto masking films, annealing after deposition of polycrystalline silicon layer, etc.

L134 ANSWER 29 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN

TI   Formation of polycide gates in integrated circuits with reduced
     delamination and bubble formation - by patterning silicide
     layer and poly:silicon on silicon@
     substrate, annealing, implanting ions, etc.

L134 ANSWER 30 OF 36 WPIX COPYRIGHT 2011   THOMSON REUTERS on STN
TI   Mfr. of photo-converters with alloyed aluminium@ contacts - includes
     forming of contact screen simultaneously on both sides of base and
     application of lithium layer onto side with phospho-
     silicate glass coating.

L134 ANSWER 31 OF 36 WPIX COPYRIGHT 2011   THOMSON REUTERS on STN
TI   Fabrication of semiconductor integrated circuits - esp MOS capacitor
     elements by forming oxide layers, dielectric layers contact holes,
     through contacts and electrodes

L134 ANSWER 32 OF 36 WPIX COPYRIGHT 2011   THOMSON REUTERS on STN
TI   Deposition of germanium-contg. layer - on oxygen-contg. insulation
     layer, by adding protection layer on insulation layer

L134 ANSWER 33 OF 36 WPIX COPYRIGHT 2011   THOMSON REUTERS on STN
TI   MIS semiconductor device - includes phosphorus doped and boron-doped
     silicon di:oxide layers, melt-recrystallised phosphorus-silicon layer,
     auto-doped region, etc.

L134 ANSWER 34 OF 36 WPIX COPYRIGHT 2011   THOMSON REUTERS on STN
TI   Thin defect free mono crystalline layer of
     semiconductor material - formed on insulators by laser zone heating
     with controlled scanning speed

L134 ANSWER 35 OF 36 WPIX COPYRIGHT 2011   THOMSON REUTERS on STN
TI   Tungsten plugs deposited in vias and contact windows - using
     deposition- and etch-back process with masking of plugs

L134 ANSWER 36 OF 36 WPIX COPYRIGHT 2011   THOMSON REUTERS on STN
TI   Semiconductor integrated circuit - comprises two
     monocrystalline silicon substrates joined
     through insulating film

=> D L134 3,8,11,20,28,29,33,34,36 FULL TT

L134 ANSWER 3 OF 36 WPIX COPYRIGHT 2011   THOMSON REUTERS on STN
AN   2004-754540 [200474]   WPIX Full-text
TI   Method for forming boro-phospho-silicate
     glass layer
DC   L03; U11
IN   KIM Y D
PA   (HYNX-C) HYNIX SEMICONDUCTOR INC
CYC 1
PI   KR 2004057636   A 20040702 (200474)* KO 1[10]

KR 557946 B1 20060310 (200724) KO [10]
ADT KR 2004057636 A KR 2002-84403 20021226; KR 557946 B1 KR 2002-84403 20021226
FDT KR 557946 B1 Previous Publ KR 2004057636 A
PRAI KR 2002-84403 20021226
AB KR 2004057636 A UPAB: 20050707

NOVELTY - A method for forming a BPSG (Boro- Phospho-Silicate Glass) layer is provided to improve insulating property by forming bubbles in the BPSG layer using ion-implantation and annealing.

DETAILED DESCRIPTION - A semiconductor substrate(1) with a gate electrode(5) is prepared. A BPSG layer(7) is formed on the resultant structure and densified by first annealing. A landing plug contact region(8) is formed by selectively etching the BPSG layer. A landing plug(9) is formed in the landing plug contact region. Bubbles are formed in the BPSG layer by performing ion-implantation and second annealing.

FS CPI; EPI
MC CPI: L04-C06C; L04-C11; L04-C12D
EPI: U11-C05B7; U11-C05G2C
TT TT: METHOD FORMING BORO PHOSPHO SILICATE GLASS LAYER

L134 ANSWER 8 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
AN 2004-069176 [200407] WPIX Full-text
CR 2001-023173
DNC C2004-028677 [200407]
DNN N2004-055615 [200407]
TI Manufacture of semiconductor structure comprises using boron and/or phosphorus-containing liquid compounds, vaporizing, directing gases toward substrate and thermally treating to form boron and/or phosphorus-containing silica layer
DC E11; E12; L03; U11
IN VAARTSTRA B A
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 20030200925 A1 20031030 (200407)* EN 9[2]
US 7273525 B2 20070925 (200764) EN
ADT US 20030200925 A1 Div Ex US 1998-146622 19980903; US 20030200925 A1 Cont of US 2000-649560 20000828; US 20030200925 A1 US 2003-436640 20030513
FDT US 20030200925 A1 Div ex US 6136703 A
PRAI US 2003-436640 20030513
US 1998-146622 19980903
US 2000-649560 20000828
AB US 20030200925 A1 UPAB: 20050528

NOVELTY - Manufacturing a semiconductor structure comprises vaporizing boron and/or phosphorus-containing liquid compounds, directing the gases toward the substrate and thermally treating the condensed liquid to form a phosphorus- and/or boron-containing silica layer on a surface of the semiconductor substrate.

DETAILED DESCRIPTION - Manufacturing a semiconductor structure comprises:

(a) using a semiconductor substrate or substrate assembly (16);

(b) using source(s) of silicon in the form of a liquid or a gas;

(c) using source(s) of a nonsilicon-containing reaction gas in the form of a liquid or a gas;

(d) using liquid compounds of the formulae B(OR3)3, P(OR4)3 and (O)P(OR5)3;

(e) vaporizing each compound provided as liquid to form gas;

(f) directing the gases toward the semiconductor substrate or substrate assembly to form a condensed liquid on a surface of the substrate or substrate assembly; and

(g) thermally treating the condensed liquid to form a phosphorus- and/or boron-containing silica layer on a surface of the semiconductor substrate or substrate assembly.

R3-R5 = alkyl or alkenyl.

An INDEPENDENT CLAIM is also included for:

(1) a chemical vapor deposition apparatus comprising:

(i) a deposition chamber having a substrate;

(ii) vessel(s) (42) containing liquid compounds of the formulae B(OR3)3, P(OR4)3 and (O)P(OR5)3;

(iii) source(s) of silicon (43) in the form of a liquid or a gas;

(iv) source(s) of a nonsilicon-containing reaction gas (48) in the form of a liquid or a gas; and

(v) optionally source(s) of an inert carrier gas (44) for transferring the liquid compounds to the chemical vapor deposition chamber;

(2) a method of manufacturing a semiconductor structure;

(3) methods of forming a silica layer on a substrate; and

(4) methods of manufacturing semiconductor structures.

USE - For manufacturing a semiconductor structure.

ADVANTAGE - The incorporation of phosphorus and/or boron allows for tailoring of the flow characteristics of the liquid Si(OH)x(O)y(H2O)z and oligomers, as well as the etching rates and dielectric constants of the resultant solid silica layers.

DESCRIPTION OF DRAWINGS - The figure shows a chemical vapor deposition system for use in the method.

Chemical vapor deposition chamber (10)

Turbo pump (12)

Backing pump (14)

Semiconductor substrate or substrate assembly (16)

Platen (18)

Vessel (42)

Silicon source (43)

Source of inert carrier gas (44)

Gas distributor (46)

Source of nonsilicon-containing reaction gas (48)

Valves (50-56)

TECH ELECTRONICS - Preferred Components: The surface of the semiconductor substrate or substrate assembly comprises small high aspect ratio openings. The semiconductor substrate comprises a silicon wafer or gallium arsenide wafer.

Preferred Method: The step of vaporizing comprises using a chemical vapor deposition technique, preferably flash vaporization, bubbling and/or microdroplet formation. The step of thermally

treating comprises exposing the condensed liquid on a surface of the substrate or substrate assembly to 200-1000 degrees C.
ORGANIC CHEMISTRY - Preferred Materials: The sources of silicon are gases, preferably silane (SiH_4). The sources of silicon may also be compounds of formula SiX_pY_{4-p}.
X = halide or H;
Y = H, R1 or OR2;
R1, R2 = organic group (preferably 1-4C alkyl or alkenyl);
p = 0-4.
The alkyl or alkenyl of R3-R5 is 1-4C alkyl or alkenyl.
INORGANIC CHEMISTRY - Preferred Materials: The sources of nonsilicon-containing reaction gas comprise oxygen (O_2), ozone (O_3), nitrous oxide (N_2O), nitric oxide (NO), water (H_2O), and/or hydrogen peroxide (H_2O_2).
CERAMICS AND GLASS - Preferred Materials: The phosphorus- and/or boron-containing silica layer is a phosphosilicate glass (PSG), borosilicate glass (BSG) or borophosphosilicate glass (BPSG).

FS   CPI; EPI
MC   CPI: E31-P06E; E31-Q08; L04-C01B; L04-C12E
     EPI: U11-C09B
TT   TT: MANUFACTURE SEMICONDUCTOR STRUCTURE COMPRISE BORON PHOSPHORUS CONTAIN LIQUID COMPOUND VAPORISE DIRECT GAS SUBSTRATE THERMAL TREAT FORM SILICA LAYER

L134 ANSWER 11 OF 36 WPIX COPYRIGHT 2011   THOMSON REUTERS on STN
AN   2003-829215 [200377]   WPIX Full-text
CR   2003-522743
DNC C2003-233401 [200377]
DNN N2003-662495 [200377]
TI   Formation of local interconnect for integrated circuitry by etching second dielectric layer selectively relative to first dielectric layer to form local interconnect outline within second dielectric layer to extend between transistors
DC   L03; U11; U12
IN   ABBOTT T R
PA   (ABBO-I) ABBOTT T R; (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI   US 20030077855 A1 20030424 (200377)* EN 17[11]

     US 6727168   B2 20040427 (200429) EN
ADT US 20030077855 A1 US 2001-1758 20011024
PRAI US 2001-1758   20011024
AB   US 20030077855 A1   UPAB: 20050531

NOVELTY - Formation of local interconnect comprises etching the second dielectric layer selectively relative to first dielectric layer to form portion of local interconnect outline within the second dielectric layer to extend between first transistor gate (20) and second transistor source/drain regions (30), the etching removing at least some of the second dielectric layer within the contact openings.

DETAILED DESCRIPTION - Formation of local interconnect comprises:

(a) providing a substrate (11) having a gate of a first transistor and a source/drain region of a second transistor;

(b) forming a first dielectric layer over the first transistor gate and the second transistor source/drain region;

(c) forming contact openings in the first dielectric layer to the first transistor gate and to the second transistor source/drain region;

(d) forming a second dielectric layer over the first dielectric layer and to within the contact openings;

(e) etching the second dielectric layer selectively relative to the first dielectric layer to form at least a portion of a local interconnect outline within the second dielectric layer to extend between the first transistor gate and the second transistor source/drain regions, the etching removing at least some of the second dielectric layer within the contact openings; and

(f) forming conductive material within the local interconnect outline within the second dielectric layer which electrically connects the first transistor gate with the second transistor source/drain region.

An INDEPENDENT CLAIM is also included for an integrated circuitry comprising a substrate having first and second transistor gate and a source/drain region; a pair of insulative sidewall spacers (24) received over the first transistor gate sidewalls, the spacers having respective uppermost surfaces (21) which are elevationally coincident with the uppermost surface of the semiconductive material; and a conductive local interconnect electrically connecting the first transistor gate silicide with the source/drain region proximate the second transistor gate.

USE - For forming local interconnect used for integrated circuitry (claimed).

ADVANTAGE - The invention incorporates gate etch with undoped polysilicon and without having to etch silicide, followed by salicidation and subsequent self-aligned contact etch.

DESCRIPTION OF DRAWINGS - The figure is a view of the wafer fragment at a processing step.

Substrate (11)
First transistor gate (20)
Uppermost surfaces (21)
Sidewall spacers (24)
Second transistor source/drain regions (30)

TECH ELECTRONICS - Preferred Method: The method further comprises forming the contact openings in the first dielectric layer by etching. It may also include forming the silicide on the first transistor gate and on the second transistor source/drain region by refractory metal layer deposition and annealing. Preferred Component: The first and second transistor source/drain regions comprise components of static random access memory cell.

INORGANIC CHEMISTRY - Preferred Material: The first dielectric layer is undoped silicon dioxide or silicon nitride. The second dielectric layer comprises silicon dioxide doped with phosphorus and/or boron. The substrate comprises bulk monocrystalline silicon, and the source/drain region comprises diffusion region formed within the bulk monocrystalline silicon.

FS CPI; EPI

MC   CPI: L04-C11; L04-C15; L04-E01
     EPI: U11-C05D3; U11-C05D4; U11-C05F1; U11-C07C3; U12-D02A
TT   TT: FORMATION LOCAL INTERCONNECT INTEGRATE CIRCUIT ETCH SECOND
         DIELECTRIC LAYER SELECT RELATIVE FIRST FORM OUTLINE EXTEND
         TRANSISTOR

L134 ANSWER 20 OF 36 WPIX COPYRIGHT 2011   THOMSON REUTERS on STN
AN   2001-647358 [200174]   WPIX Full-text
DNC C2001-190993 [200174]
DNN N2001-483642 [200174]
TI   Manufacture of stencil mask by defining opening locations in
     substrate, providing dopant in substrate, forming openings in opening
     locations, providing additional dopant, and forming stencil mask
DC   G06; P84
IN   BERRY I L; ROLFSON J B
PA   (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI   US 6300017   B1 20011009 (200174)* EN 11[9]
ADT US 6300017 B1 US 1998-137504 19980820
PRAI US 1998-137504   19980820
AB   US 6300017 B1   UPAB: 20050527

NOVELTY - A stencil mask is made by defining opening locations in a substrate; providing dopant in the substrate to form dopant-concentrated first regions, each surrounding an opening location, and second region(s) less concentrated with the dopant; forming openings in the opening locations; providing a different additional dopant at least in the first regions; and forming the stencil mask.

DETAILED DESCRIPTION - Manufacture of a stencil mask includes defining opening locations within a substrate (32). A dopant is provided in the substrate to form first regions (40) concentrated with the dopant and second region(s) less concentrated with the dopant. Each first region surrounds an opening location. The dopant has a conductivity type similar to the background dopant in the substrate. Openings (42) extending to the substrate are formed within the opening locations. A different additional dopant is provided at least in the first regions. The stencil mask comprising at least a portion of the first and second regions is then formed.

USE - For manufacturing stencil masks used in patterning a resist coated target in ion and electron beam lithography.

ADVANTAGE - The dopants create forces that prevent structural deformations e.g. bowing, of the openings.

DESCRIPTION OF DRAWINGS - The drawing shows a step in manufacturing stencil mask.

Substrate (32)
First regions (40)
Openings (42)

TECH ELECTRONICS - Preferred Method: The openings can be formed before providing the dopant. A patterned material covers portion(s) of the substrate. Dopant is provided in the uncovered substrate portions, and is driven beneath the patterned material. The uncovered portions are removed, forming the openings. The dopant is provided by forming a liquid layer comprising the dopant on the substrate, solidifying the

liquid layer, and diffusing the dopant from the solidified layer to the substrate. The dopant can be provided by gas phase doping. The dopant is driven by thermal treatment of the substrate to diffuse the dopant in the semiconductive material. The patterned material is removed from the substrate. Preferred Components: The substrate comprises a semiconductive material. The second regions do not comprise the dopant. The patterned material comprises a photoresist layer. The pattern dopant is n-type or p-type. The additional dopant is n-type. Preferred Parameters: The dopant concentration is at least 1017 atoms/cm3. The dopant has atomic radii smaller or bigger than that of the substrate material.
INORGANIC CHEMISTRY - Preferred Materials: The substrate comprises monocrystalline silicon. The patterned material comprises silicon dioxide layer. The pattern dopant comprises boron or phosphorus.

FS CPI; GMPI
MC CPI: G06-D01; G06-D03; G06-D06; G06-E02
TT TT: MANUFACTURE STENCIL MASK DEFINE OPEN LOCATE SUBSTRATE DOPE FORMING ADD

L134 ANSWER 28 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
AN 1997-010214 [199701] WPIX Full-text
DNC C1997-002556 [199701]
DNN N1997-009137 [199701]
TI Mfr. of insulation elements of integrated circuits - includes additional deposition of phosphor or borosilicate glass onto masking films, annealing after deposition of polycrystalline silicon layer, etc.
DC L03; U11; U13
IN KOKIN V N; MANZHA N M; YACHMENEV V V
PA (MANZ-I) MANZHA N M
CYC 1
PI SU 1111634 A1 19960410 (199701)* RU 6[8]
ADT SU 1111634 A1 SU 1982-3501668 19821020
PRAI SU 1982-3501668 19821020***
AB SU 1111634 A1 UPAB: 20050514
A concealed layer (2) with surface resistance of 25 - 35 ohms / cm. is formed in a ***monocrystalline silicon substrate (1) of p-type conductivity and an epitaxial silicon film (3) of n-type conductivity is grown with resistance of 0.8 - 1.5 ohm / cm. and thickness of 1.2 - 3.0 μm. Film (3) is oxidised thermally to obtain a silicon dioxide film (4) and a silicon nitride film (5) is applied by a vacuum pyrolysis method. A film (6) of phosphor-silicate glass is then deposited by pyrolysis in a gas carrier flow.
Channels with depths of 4.2 - 7.0 μm are etched, silicon dioxide films are formed on the walls and bottoms of the channels and anti-channels areas are formed on the bottoms of the channels by implantation of boron ions. A polycrystalline silicon layer is applied and the structure is annealed at 1000 °C in argon or nitrogen

for 30 - 40 mins, to oxidise the silicon, before collector, base and emitters areas of transistors are formed.

USE - Mfr. of insulation of elements of super-large integrated circuits.

ADVANTAGE - Increased number of integrated circuits by improved design.

ABDT SU1111634

A concealed layer (2) with surface resistance of 25 - 35 ohms / cm. is formed in a monocrystalline silicon substrate (1) of p-type conductivity and an epitaxial silicon film (3) of n-type conductivity is grown with resistance of 0.8 - 1.5 ohm / cm. and thickness of 1.2 - 3.0 μm. Film (3) is oxidised thermally to obtain a silicon dioxide film (4) and a silicon nitride film (5) is applied by a vacuum pyrolysis method. A film (6) of phosphor-silicate glass is then deposited by pyrolysis in a gas carrier flow.

Channels with depths of 4.2 - 7.0 μm are etched, silicon dioxide films are formed on the walls and bottoms of the channels and anti-channels areas are formed on the bottoms of the channels by implantation of boron ions. A polycrystalline silicon layer is applied and the structure is annealed at 1000 °C in argon or nitrogen for 30 - 40 mins, to oxidise the silicon, before collector, base and emitters areas of transistors are formed.

USE

Mfr. of insulation of elements of super-large integrated circuits.

ADVANTAGE

Increased number of integrated circuits by improved design.

FS CPI; EPI

MC CPI: L04-C12A; L04-C12B; L04-C12D; L04-C16
EPI: U11-C08A3; U13-C06

TT TT: MANUFACTURE INSULATE ELEMENT INTEGRATE CIRCUIT ADD DEPOSIT PHOSPHOR BOROSILICATE GLASS MASK FILM ANNEAL AFTER POLYCRYSTALLINE SILICON LAYER

L134 ANSWER 29 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN

AN 1995-263250 [199534] WPIX Full-text

TI Formation of polycide gates in integrated circuits with reduced delamination and bubble formation - by patterning silicide layer and poly:silicon on silicon@ substrate, annealing, implanting ions, etc.

DC L03; U11

IN CHANG T C; CHU C; HUANG H; HWANG S; JANG T; JU C; LIAW Y

PA (TSMC-C) TAIWAN SEMICONDUCTOR MFG CO LTD

CYC 2

PI US 5434096 A 19950718 (199534)* EN 7[4]
TW 291574 A 19961121 (199712) ZH

ADT US 5434096 A US 1994-318212 19941005; TW 291574 A TW 1995-101973 19950302

PRAI US 1994-318212 19941005

AB US 5434096 A UPAB: 20050702

Manufacture of an integrated circuit comprises (a) providing on a silicon substrate a polysilicon layer over a gate dielectric; (b) forming a silicide layer and patterning it and the polysilicon to form a pattern of gate electrodes;. (c) annealing the substrate in an inert atmosphere and then oxygen; (d) performing lightly dopes source/drain ion implants into the substrate; (e) forming spacers on the sidewalls of the polycide gate electrodes; (f) performing source/drain ion implants into the substrate; (g) degassing the substrate in inert atmosphere; (h) depositing a dielectric layer over the polycide gate electrode pattern and flowing the dielectric to complete the circuit.

USE - Fabrication of polycide gates.

ADVANTAGE - Delamination after BPSG flow is prevented. ABDT US5434096

Manufacture of an integrated circuit comprises

(a) providing on a silicon substrate a polysilicon layer over a gate dielectric;

(b) forming a silicide layer and patterning it and the polysilicon to form a pattern of gate electrodes;

(c) annealing the substrate in an inert atmosphere and then oxygen;

(d) performing lightly dopes source/drain ion implants into the substrate;

(e) forming spacers on the sidewalls of the polycide gate electrodes;

(f) performing source/drain ion implants into the substrate;

(g) degassing the substrate in inert atmosphere;

(h) depositing a dielectric layer over the polycide gate electrode pattern and flowing the dielectric to complete the circuit.

USE

Fabrication of polycide gates.

ADVANTAGE

Delamination after BPSG flow is prevented.

EXAMPLE

WSi_x was formed at 300°C, patterning was by conventional lithography and anisotropic etching. The dielectric spacer was 2000-3000 Å of CVD SiO_2 . The dose of BF_2 was 1-5 E15ohms/cm 2 and 50-100 Kev for N^+ the dose is As. The degassing for 20 mins at >800°C removes fluorine gas and reduces delamination. The dielectric in Step 8 was BPSG or BPTEOS at 3-11000 Å. (KB)

PREFERRED METHOD

The silicide layer is formed using WF_6 and SiH_4 to form tungsten silicide. Annealing is carried out in >850°C of 10-300 min in oxygen. The source/drain implants use BF_2 ions and degassing to at >800°C in nitrogen, argon or vacuum. The dielectric is boro phosphosilicate glass and on underlayer of undoped silicate glass and the layer is flowed at 850-1000 °C.

FS CPI; EPI

MC CPI: L04-C02B; L04-C10B; L04-C11C; L04-C16; L04-C26
EPI: U11-C05B9; U11-C05D1; U11-C18A3

TT TT: FORMATION POLYCIDE GATE INTEGRATE CIRCUIT REDUCE DELAMINATE BUBBLE PATTERN SILICIDE LAYER POLY SILICON SILICON@ SUBSTRATE ANNEAL IMPLANT ION

L134 ANSWER 33 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN

AN 1989-239252 [198933] WPIX Full-text
DNC C1989-106864 [199216]
DNN N1989-182124 [199216]
TI MIS semiconductor device - includes phosphorus doped and boron-doped
silicon di:oxide layers, melt-recrystallised phosphorus-silicon layer,
auto-doped region, etc.
DC L03; U11; U12; U13
IN FUNAHASHI T; KUROYANAGI A
PA (NPDE-C) NIPPONDENSO CO LTD
CYC 1
PI JP 01175262 A 19890711 (198933)* JA 6[6]
JP 2545903 B2 19961023 (199647) JA 5[0]
ADT JP 01175262 A JP 1987-332689 19871229; JP 2545903 B2 JP
1987-332689 19871229
FDT JP 2545903 B2 Previous Publ JP 01175262 A
PRAI JP 1987-332689 19871229
AB JP 01175262 A UPAB: 20050428
Semiconductor device comprises silicon substrate, intermediate insulation film, phosphorus doped silicon dioxide (PSG) film, boron doped silicon dioxide (BSG) film, molten recrystallised P-silicon layer,P-autodoped region formed on the P-silicon layer by auto doping boron into the P-silicon layer from the BSG film, gate insulation film on the surface of the P-silicon layer, gate electrode,and N-source region and N-drain region whose mutual continuity is controlled by the gate electrode formed on the surface of the P-silicon layer.
USE/ADVANTAGE - MIS semiconductor device can be melted and recrystallised on insulation film using laser or lamp.
FS CPI; EPI
MC CPI: L04-C02; L04-C04
EPI: U11-C01J8; U11-C03J1; U11-C08A5; U12-D02A; U13-D
TT TT: MIS SEMICONDUCTOR DEVICE PHOSPHORUS DOPE BORON SILICON DI OXIDE
LAYER MELT RECRYSTALLISATION AUTO REGION
AW: METAL INSULATE SEMICONDUCTOR

L134 ANSWER 34 OF 36 WPIX COPYRIGHT 2011 THOMSON REUTERS on STN
AN 1988-147218 [198821] WPIX Full-text
DNC C1988-065614 [199321]
DNN N1988-112414 [199321]
TI Thin defect free mono crystalline layer of
semiconductor material - formed on insulators by laser zone heating
with controlled scanning speed
DC L03; U11
IN MARTINEZ A M; PANDYA R
PA (PHIG-C) N AMER PHILIPS CORP
CYC 7
PI US 4743567 A 19880510 (198821)* EN 5[3]
EP 303320 A 19890215 (198907) EN
JP 01066929 A 19890313 (198916) JA
ADT US 4743567 A US 1987-84657 19870811; EP 303320 A EP
1988-201666 19880802; JP 01066929 A JP 1988-197276
19880809
PRAI US 1987-84657 19870811

AB   US 4743567 A   UPAB: 20060105
      A thin defect free monocrystalline layer of Si on an insulator is formed by (i) deposition of a thin (less than 10 micron thick) polycrystalline or amorphous layer of Si on a glass substrate, pref. phosphosilicate glass, borophosphosilicate glass, aluminosilicate glass or spin on glass; (ii) heating using a zone heating source to provide a convex solid/liq. interface in Si layer; and (iii) scanning the heating source at less than 1 mm/sec., and maintaining the substrate at its annealing pt. to move the solid/liq. interface along Si layer, while surface of substrate opposite to Si layer is liquified under convex solid/liq. interface.

      USE/ADVANTAGE - The formation of thin defect free monocrystalline layers of Si on insulators with the distance between the low angle grain boundaries significantly increased.

FS   CPI; EPI

MC   CPI: L04-B02; L04-C18
      EPI: U11-C01J8; U11-C03C; U11-C03J1; U11-C03J5

TT   TT: THIN DEFECT FREE MONO CRYSTAL LAYER SEMICONDUCTOR MATERIAL FORMING INSULATE LASER ZONE HEAT CONTROL SCAN SPEED

L134 ANSWER 36 OF 36 WPIX COPYRIGHT 2011   THOMSON REUTERS on STN

AN   1978-90470A [197850]   WPIX Full-text

TI   Semiconductor integrated circuit - comprises two monocrystalline silicon substrates joined through insulating film

DC   L03; U11; U12; U13

IN   FUJIMOTO Y; KUSAKA T; TSUJIIDE T

PA   (NIDE-C) NIPPON ELECTRIC CO

CYC   1

PI   JP 53128285   A 19781109 (197850)* JA

ADT   JP 53128285 A JP 1977-43256 19770414

PRAI JP 1977-43256   19770414

AB   JP 53128285 A   UPAB: 20050417
      The semiconductor integrated circuit structure comprises a first substrate and a second substrate consisting of single crystalline silicon, the second substrate being joined with the first substrate through an insulating film, circuit elements being formed in the second substrate. The first substrate may consist of single crystalline silicon.

      The structure is fabricated by preparing first and second single crystalline silicon substrates with silicon oxide films and phosphor silicate glass or borosilicate glass films respectively, joining these two substrate through a glass layer formed by fusing together the two glass films, thinning the first silicon substrate, and forming circuit elements in the thinned silicon substrate. Prodn. is easier than when using an SOS technique.

FS   CPI; EPI

MC   CPI: L03-D04

TT   TT: SEMICONDUCTOR INTEGRATE CIRCUIT COMPRISE TWO MONOCRYSTAL SILICON SUBSTRATE JOIN THROUGH INSULATE FILM